Philips RF Manual

product & design manual for
RF small signal discretes

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APPENDIX

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Content appendix:

Application notes:

Appendix A 2.4GHz Gen. Front-End Demoboard

1.1. Introduction

1.1.1. Description of a generic Front-End

This document describes a demoboard for the upcoming 2.4GHz Industrial-Scientific-Medical ***(ISM)*** band for applications like wireless communication, LAN and video/TV signal transmission. It covers a power amplifier ***(PA)*** for transmitting, a low noise amplifier ***(LNA)*** for receiving and an RF switch for multiplexing these two main circuits to a third antenna terminal. This document illustrates applications information, standards, description of the board itself and a selection of the design procedure. Modern IC processes make it possible to integrate the main receiver ***(RX)*** and transmitter ***(TX)*** functions into a one-chip solution. The actual highly integrated circuits ***(IC)*** doesn't reach the receiver front-end performance of noise and linearity compared with an LNA implemented by an optimised discrete transistor or Monolithic Microwave Integrated Circuit ***(MMIC)***. Due to thermal radiation limitations of the IC package, only low output transmission power is supported. These IC limitations do reduce the receiver sensitivity itself and the RF power arrival at the other RF-link member. The practical result is a shorter distance between the users. This 2.4GHz generic front-end demoboard was deigned for improving the IC's noise and output power for expanded operation distance. The following diagram illustrates the front-end board working together with a transmitter IC. This general front-end is not designed for a specific application or standard.

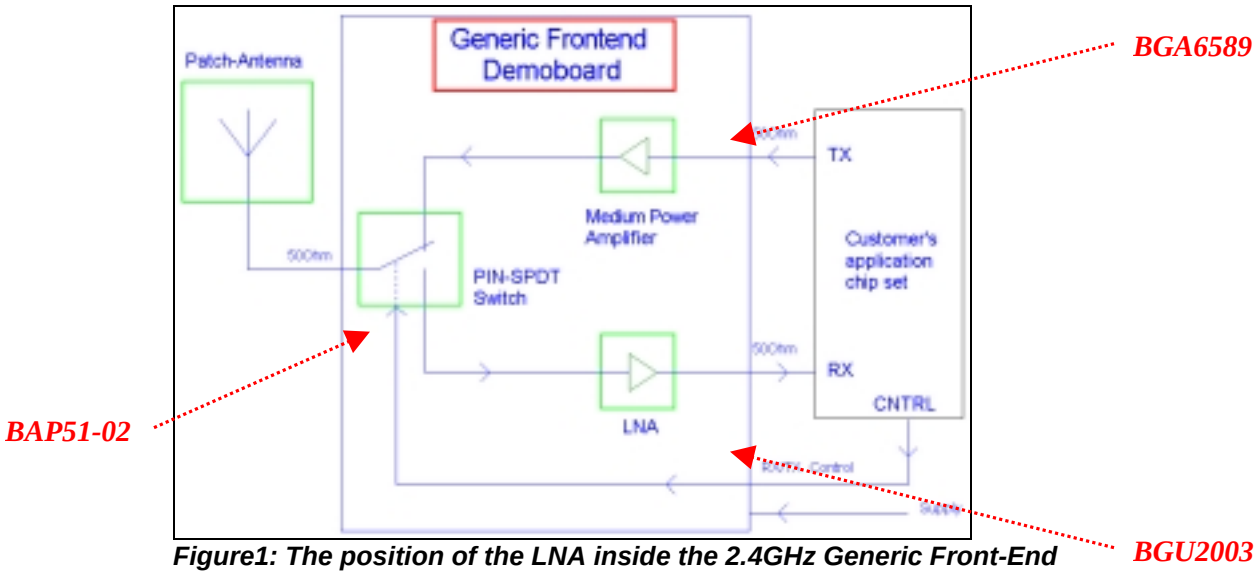


Figure1: The position of the LNA inside the 2.4GHz Generic Front-End

- ***The job of the Front-End in an application***

The demoboard supports half duplex operation. This means the TX and RX operation are possible, but, not at the same time. The time during Transmission ***(TX)*** activity and Receiving ***(RX)*** activity are so called ***time slots*** or just ***slots***. The order of the TX and RX time slots is specific for the application standard. Special application transmission activities consist of several TX and RX slots put together in the so called ***time-frame*** or short just a ***frame***. The ***user points*** / ***access points*** with this kind of wireless application must follow the same functionality of slots, same order of frames and timing procedure ***(synchronisation)***. These kind of issues must be under the control of specific rules normally defined by specific ***Institutes*** or ***Organisation*** like ETSI, IEEE, NIST, FCC, CEPT, and so on.

- ***How does the Front-End work?***

Under the control (CNTRL-Pin) of customer's chip set, the Front-End ***SPDT*** (single pole double through) Switch based on the ***PIN Diode BAP51-02*** closes the path between the antenna and the Medium Power Amplifier in the TX time slot. The output power signals can be radiated from the antenna away into the Ether/Space. The ***Ether*** is the natural environment medium around being used by the wireless RF travelling waves from one access point to the other one. Because the TX signals are amplified by the ***Medium Power Amplifier BGA6589,*** more powerful signals can be transmitted and reach further distances.

The signal receiving occurs during the RX time slot. For this operation mode, the antenna is switched away from the **PA** (power amplifier) and connected to the LNA input under the control of the CNTRL-Pin. System analysis of the noise performance of a complete receiver show that a ***low noise amplifier (LNA) BGU2003*** can improve the receiver sensitivity by reduction the effective RX system noise figure ***(NF)***. This is done by installing moderate gain with very low noise in the front of the noisy IC receiver input by the use of the LNA. The effect is the receiver's ability to properly receive signals from access points at much further distances. This effect can be shown by the mathematical relationship shown below :

With the general Noise Figure **(NF)** definition: $NF = 10 \cdot \log(F) = 10\log\left(\frac{Pout_{Noise}}{Pin_{Noise}}\right)$. All the time, the amount of the noise ratio F will be larger than one (*F>1 or NF>0dB*) for operating at temperature larger than zero degree Kelvin.

The overall System Noise Ratio of the cascade LNA + RX chip results in: $F_{SYST} = F_{LNA} + \frac{F_{RX} - 1}{Gain_{LNA}}$. The F_{SYST} illustrates that the overall system noise ratio (LNA+RX chip set) is at least the F_{LNA}. There is the addition of a second amount of noise caused by the ICs RX channel. But this amount is reduced by the LNA gain $Gain_{LNA}$. Use of moderate LNA does reduce the noise ratio part of the receiver chip set. In this kind of relationship the LNA's noise ratio F_{LNA} is dominant.

Example-1:

- *Issue:* Customer's receiver chip-set with a NF=9dB; LNA with Power Gain=13dB and NF=1.3dB
- *Question:* What's the amount of the system receiver's noise figure?
- *Calculation:*

$$Gain_{LNA} = 10^{\frac{13dB}{10}} = 20$$

$$F_{RX} = 10^{\frac{9dB}{10}} = 7.943$$

$$F_{LNA} = 10^{\frac{1.3dB}{10}} = 1.349$$

LNA-noise part

Reduced RX chip-set noise part

$$F_{SYST} = F_{LNA} + \frac{F_{RX} - 1}{Gain_{LNA}} = 1.349 + \frac{7.943 - 1}{20} = 1.349 + 0.347$$

$$F_{SYST} = 1.696$$

$$NF_{SYST} = 10\log(F_{SYST}) = 10\log(1.696)$$

$$NF_{SYST} = 2.3dB$$

- *Answer:* In this example the use of the LNA in front of the receiver chip-set does improve the overall receiver system noise figure to NF=2.3dB. The equations show that the first device in a cascade of objects has the most effect on the overall noise figure. In reality the first part of a receiver is the antenna. Its quality is very important.

Example-2:

Philips Medium Power MMICs portfolio offer the following listed insertion power gain $|S_{21}|^2$ performances:

BGA6289 12dB

BGA6589 15dB

- *Question:*

What is the expected approximated increase of distance using this Philips' MMICs negating the attenuation of the Ether from an antenna with 3D homogenous round around field radiation in front of the chip-set?

- *Calculation:*

3D homogenous round around radiation power is general done by an ideal spherical dot. The theoretical reference isotropic antenna's travelling damped wave power-density radiation is described by the general Physical law:

$$P_{E(r)} = P_S \cdot A_E \cdot \frac{1}{4\pi \cdot r^2} \cdot e^{-\chi \cdot r}$$

$P_{E(r)}$ = Receiver power in the distance "r" to the transmitter's isotropic antenna

r = Distance receiver-transmitter

P_S = Transmitter power

χ = Atmospheric attenuation exponent

A_E = Receiver antenna surface

This kind of general Physic's law is used for all kinds of spherical wave and energy radiation topics like in optics, acoustics, thermal, electromagnetic and so on. The job of the electromagnetic wave radiating antenna is the power matching of the cable impedance (50Ω, 75Ω,...) to the space's impedance with the (ideal) electromagnetic far field impedance of 120πΩ. The received normalised power/unit area P_r at the receiver transmitted from a transmitter with the power P_t in the distance d and neglecting of atmospheric attenuation (χ=0) is calculated by: $P_{RX} = \frac{P_{TX}}{4\pi \cdot d^2}$

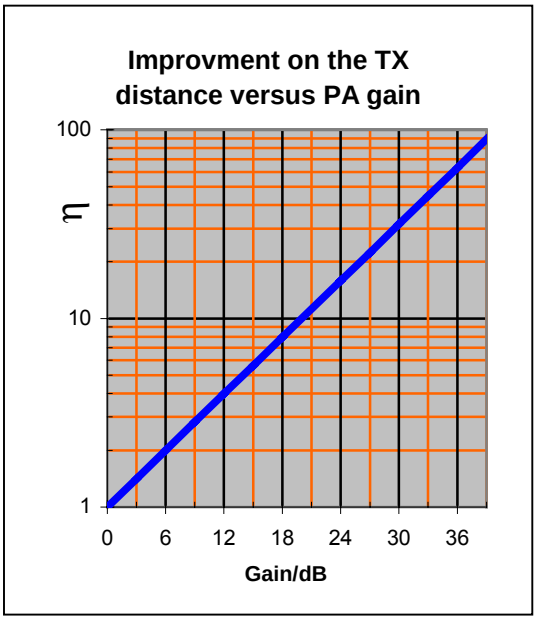
TX-RX-distance: $d = \sqrt{\frac{P_t}{4\pi \cdot P_r}}$ without PA: $d_1 = \sqrt{\frac{P_{t1}}{4\pi \cdot P_r}}$

Expanded distance by the PA for same received RX power: $d_2 = \sqrt{\frac{P_{t2}}{4\pi \cdot P_r}}$

$$\eta = \frac{d_2}{d_1} = \frac{\sqrt{\frac{P_{t2}}{4\pi \cdot P_r}}}{\sqrt{\frac{P_{t1}}{4\pi \cdot P_r}}} = \sqrt{|S21|^2} \qquad \eta = \sqrt{|S21|^2}$$

BGA6289 gain factor: $10^{\frac{12dB}{10}} = 15.85$ BGA6589 gain factor: $10^{\frac{15dB}{10}} = 31.62$

$\eta_{BGA6289} = \sqrt{15.85} = 3.98$ $\eta_{BGA6589} = \sqrt{31.62} = 5.62$



- *Answer:*

Use of BGA6289 can theoretical increase the transmitter operation area by the factor of 4. The BGA6589 can increase the operation area by 5.6 assuming no compression of the amplifiers and an isotropic antenna radiator. In reality we have to take into account the amplifier input/output matching circuits adding or removing of gain to device's insertion power gain, the frequency depending attenuation of the Ether and the gain of the receiver and transmitter antenna.

1.1.2. Applications for the demoboard

Some application ideas for the use of the Generic Front-End Demoboard

- 2.4GHz WLAN
- Wireless video, TV and remote control signal transmission
- PC to PC data connection
- PC headsets
- PC wireless mouse, key board, and printer
- Palm to PC, Keyboard, Printer connectivity
- Supervision TV camera signal transmission
- Wireless loudspeakers
- Robotics
- Short range underground walky-talky
- Short range snow and stone avalanche person detector
- Key less entry
- Identification
- Tire pressure systems
- Garage door opener
- Remote control for alarm-systems
- Intelligent kitchen (cooking place, Microwave cooker and washing machine operator reminder)
- Bluetooth
- DSSS 2.4GHz WLAN (IEEE802.11b)
- OFDM
- 2.4GHz WLAN (IEEE802.11g)
- Access Points
- PCMCIA
- PC Cards
- 2.4GHz Cordless telephones
- Wireless pencil as an input for Palms and PCs
- Wireless hand scanner for a Palm
- Identification for starting the car engine
- Wireless reading of gas counters
- Wireless control of soft-drink /cigarette/snag - SB machine
- Communication between bus/taxi and the stop lights
- Panel for ware house stock counting
- Printers
- Mobiles
- Wireless LCD Display
- Remote control
- Cordless Mouse
- Automotive, Consumer, Communication

Please note:
The used MMICs and PIN diodes can be used in other frequency ranges e.g. 300MHz to 3GHz for applications like communication, networking and ISM too.

1.1.3. The demoboard together with Philips ICs

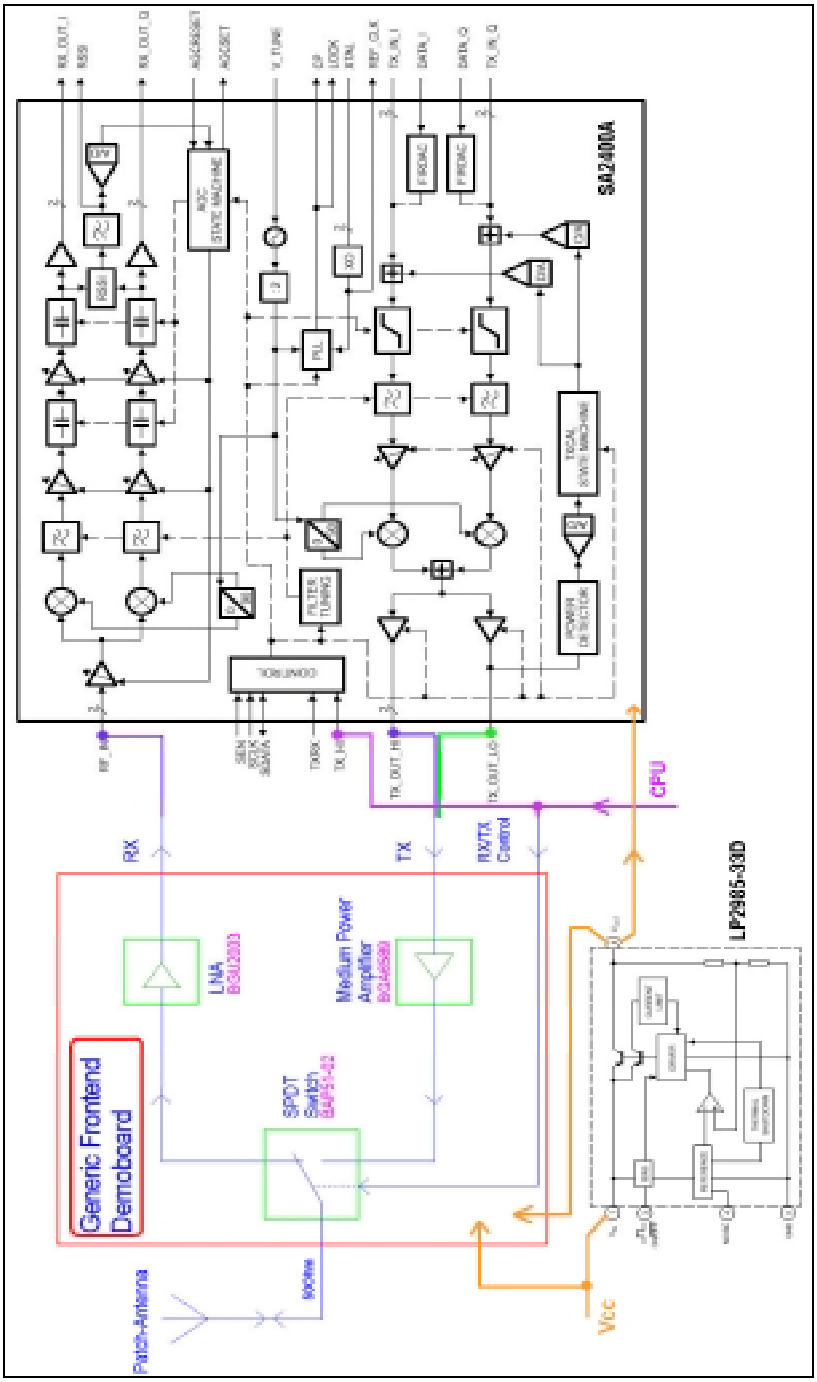


Figure 2: The Generic Front-End together with Philips' SA2400A for 2.45 GHz ISM band

Illustrated is a principle idea how the 2.4GHz Generic Front-End demoboard can work together with a transceiver for improved performances.

Up and down direct conversion I/Q transmitter for 2.4GHz with TX output power up to +20dBm and RX low noise. Digital control of all functions.

Main devices from Philips Semiconductors:

- BGU2003
- BGA6589
- BAP51-02
- SA2400A
- LP2985-33D

1.1.4. Selection of Application Regulations

Application	*Standardisation name/ issue*	*Start frequency*	*Stop Frequency*	*Centre frequency*	*Bandwidth-MHz/ Channel Spacing-MHz*
Bluetooth	IEEE802.15.1	NUS/EU=2402 (All)=2402	NUS/EU=2480 (All)=2495	2442.5MHz	NSU/EU=78/1MHz (All)=93/1MHz
DECT@ISM	ETSI	2400 MHz	2483 MHz	2441.5MHz	83/
ZigBee	IEEE802.15.4	US=2402 EU=2412	US=2480 EU=2472		US=83/4MHz EU=60/4
USA - ISM		2400MHz	2483.5GHz	2441.75MHz	83.5/
Wireless LAN; 2Mbps	IEEE802.11	2400 MHz	2483 MHz	2441.5MHz	83/FHSS=1MHz; DSSS=25MHz
Wireless LAN; 11Mbps	IEEE802.11b	2412MHz	2462MHz	2437MHz	56/
Wireless LAN; 54Mbps	IEEE802.11g				
WPLAN	NIST	2400MHz			
Fixed Mobile; Amateur; Amateur Satellite; ISM, SRD, RLAN, RFID	ERC, CEPT Band Plan	2400MHz	2450MHz	2425MHz	50/
Fixed RF transmission	acc. CEPT Austria regulation	2400MHz	2450MHz	2425MHz	50/
MOBIL RF; SRD	acc. CEPT Austria regulation	2400MHz	2450MHz	2425MHz	50/
Amateur Satellite		2400MHz	2450MHz	2425MHz	50/
Amateur	FCC	2390MHz	2450MHz		60/
UoSAT-OSCAR 11 Telemetry	Amateur Radio Satellite UO-11			2401.5MHz	
AMSAT-OSCAR 16	Amateur Radio Satellite AO-16			2401.1428MHz	
DOVE-OSCAR 17	Amateur Radio Satellite DO-17			2401.2205MHz	
Mobile LEO Satelite					
HomeRF; SWAP/CA		NUS/EU=2402 (All)=2402	NUS/EU=2480 (All)=2495		78/1MHz, 3.5MHz 93/1MHz, 3.5MHz

Abbreviations: European Radio communication Committee **(ERC)** within the European Conference of Postal and Telecommunication Administration **(CEPT)**

NIST	=	National Institute of Standards and Technology
WPLAN	=	Wireless Personal Area Networks
WLAN	=	Wireless Local Area Networks
ISM	=	Industrial Scientific Medical
LAN	=	Local Area Network
IEEE	=	Institute of Electrical and Electronic Engineers
SRD	=	Short Range Device
RLAN	=	Radio Local Area Network
RFID	=	Radio Frequency Identification
OSCAR	=	Orbit Satellite Carry Amateur Radio
FHSS	=	Frequency Hopping Spread Spectrum
DSSS	=	Direct Sequence Spread Spectrum
DECT	=	Digital Enhanced Cordless Telecommunications
NUS	=	North America
EU	=	Europe
ITU	=	International Telecommunications Union
ITU-R	=	ITU Radio communication sector

1.2. Summary

1.2.1. Block Diagram

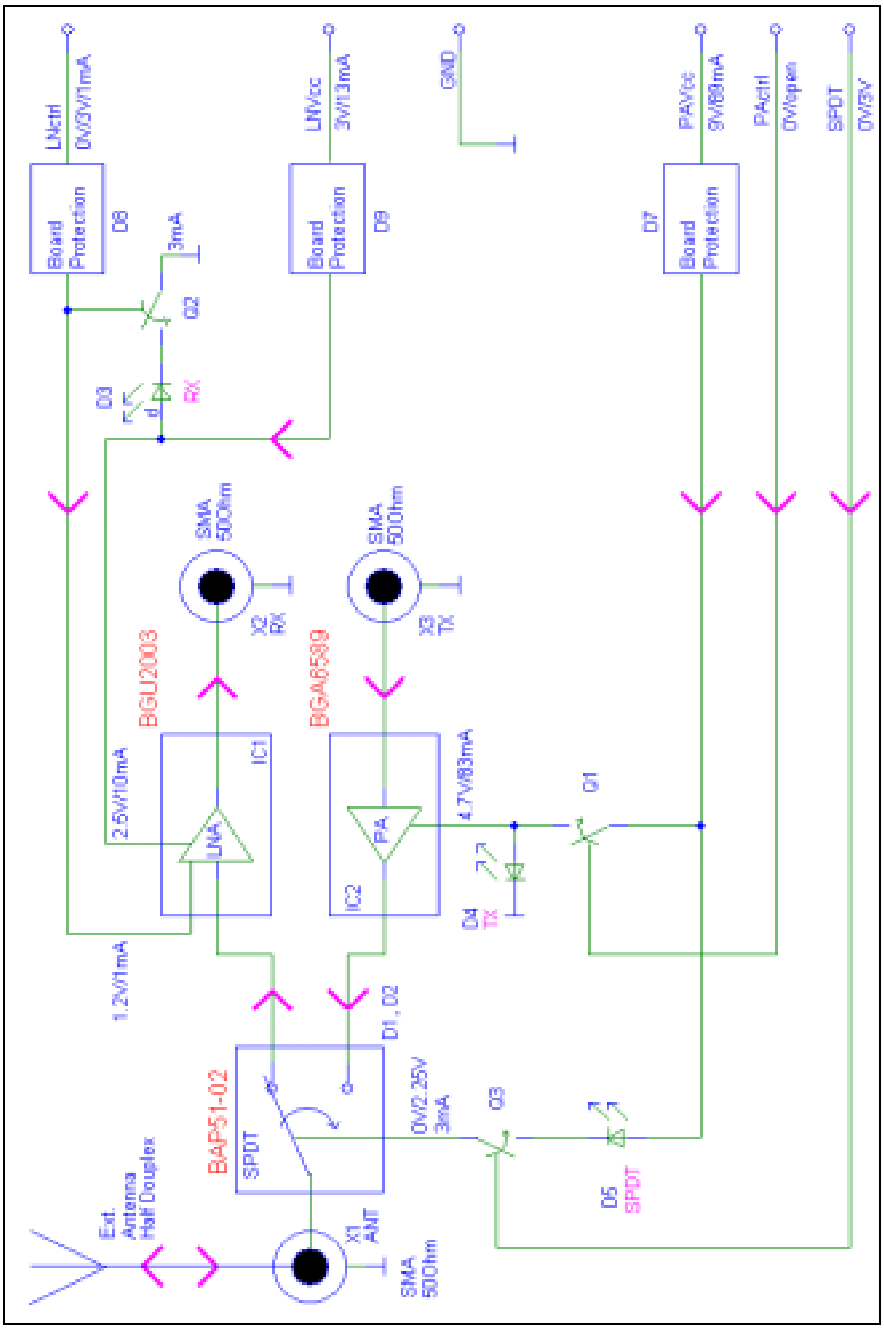


Figure 3: Block Diagram of the Demoboard

1.2.2. Schematic

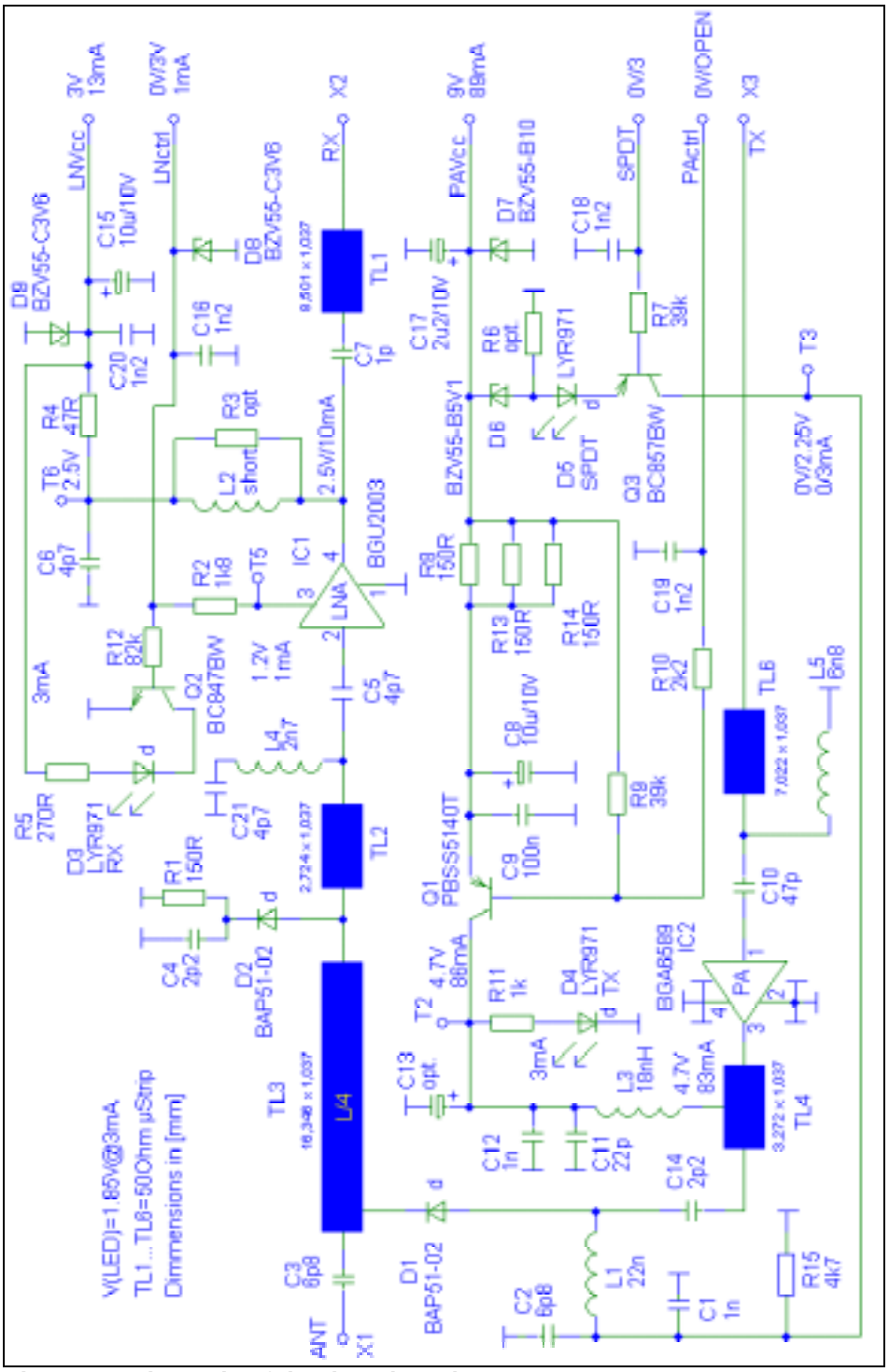


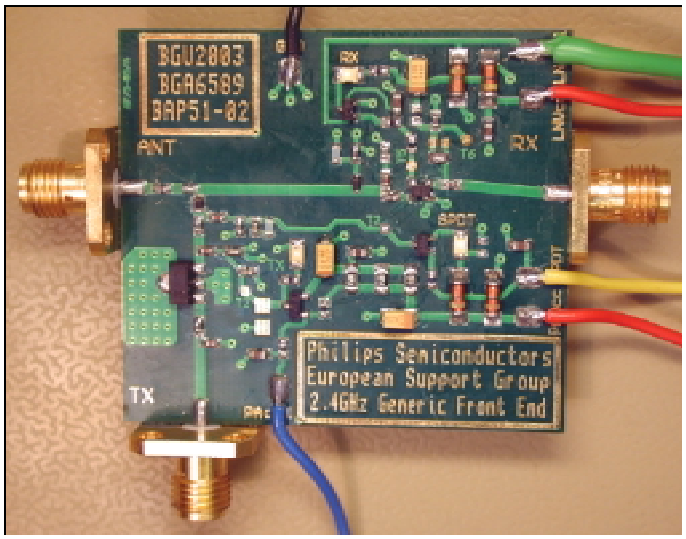
Figure 4: Schematic of the demoboard

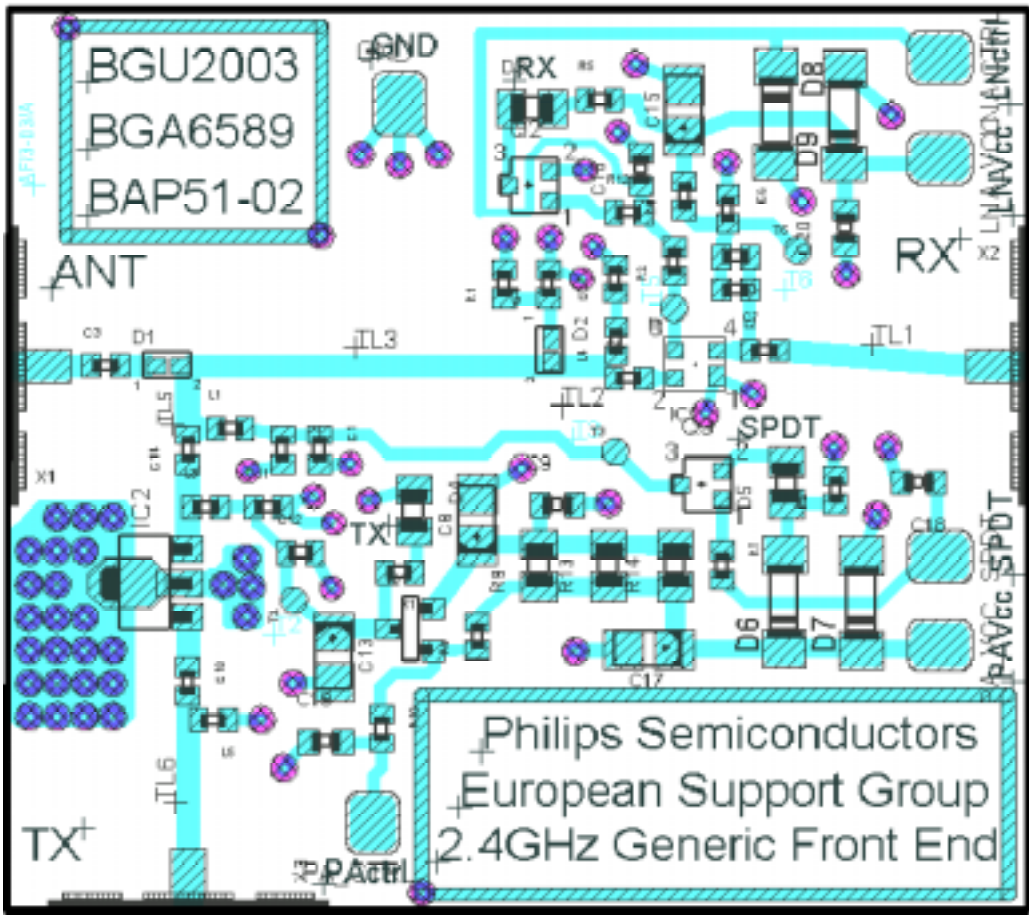
1.2.3. Part List

Part Number	Value	Size	Function / Short explanation	Manufacturer	Order Code	Order source
IC1	BGU2003	SOT363	LNA-MMIC	Philips Semiconductors	BGU2003	PHL
IC2	BGA6589	SOT89	TX-PA-MMIC	Philips Semiconductors	BGA6589	PHL
Q1	PBSS5140T	SOT23	TX PA-standby control	Philips Semiconductors	PBSS5140T	PHL
Q2	BC847BW	SOT323	LNA MMIC active	Philips Semiconductors	BC847BW	PHL
Q3	BC857BW	SOT323	SPDT switching (NPN/PNP double transistor)	Philips Semiconductors	BC857BW	PHL
D1	BAP51-02	SOD523	SPDT-TX; series PIN	Philips Semiconductors	BAP51-02	PHL
D2	BAP51-02	SOD523	SPDT-RX; shunt PIN	Philips Semiconductors	BAP51-02	PHL
D3	LYR971	0805	LED, yellow, RX	OSRAM	67S5126	Bürklin
D4	LYR971	0805	LED, yellow; TX	OSRAM	67S5126	Bürklin
D5	LYR971	0805	LED, yellow; SPDT; voltage level shifter	OSRAM	67S5126	Bürklin
D6	BZV55-B5V1	SOD80C	Level shifting for being 3V/5V tolerant	Philips Semiconductors	BZV55-B5V1	PHL
D7	BZV55-B10	SOD80C	Board DC polarity & over voltage protection	Philips Semiconductors	BZV55-B10	PHL
D8	BZV55-C3V6	SOD80C	Board DC polarity & over voltage protection	Philips Semiconductors	BZV55-C3V6	PHL
D9	BZV55-C3V6	SOD80C	Board DC polarity & over voltage protection	Philips Semiconductors	BZV55-C3V6	PHL
R1	150Ω	0402	SPDT bias	Yageo RC0402 Vitrohm512	26E558	Bürklin
R2	1k8	0402	LNA MMIC current CTRL	Yageo RC0402 Vitrohm512	26E584	Bürklin
R3	optional	0402	L2 resonance damping; optional		optional	
R4	47Ω	0402	LNA MMIC collector bias	Yageo RC0402 Vitrohm512	26E546	Bürklin
R5	270Ω	0402	LED current adj.	Yageo RC0402 Vitrohm512	26E564	Bürklin
R6	optional	0402				
R7	39k	0402	Q3 bias SPDT	Yageo RC0402 Vitrohm512	26E616	Bürklin
R8	150Ω	0805	PA-MMIC collector current adjust and temperature compensation	Yageo RC0805 Vitrohm503	11E156	Bürklin
R9	39k	0402	Helps switch of f of Q1	Yageo RC0402 Vitrohm512	26E616	Bürklin
R10	2.2kΩ	0402	Q1 bias PActrl	Yageo RC0402 Vitrohm512	26E586	Bürklin
R11	1kΩ	0402	LED current adjust; TX-PA	Yageo RC0402 Vitrohm512	26E578	Bürklin
R12	82k	0402	Q2 drive	Yageo RC0402 Vitrohm512	26E624	Bürklin
R13	150Ω	0805	PA-MMIC collector current adjust	Yageo RC0805 Vitrohm503	11E156	Bürklin
R14	150Ω	0805	PA-MMIC collector current adjust	Yageo RC0805 Vitrohm503	11E156	Bürklin
R15	4k7	0402	Improvement of SPDT-Off	Yageo RC0402 Vitrohm512	26E594	Bürklin
L1	22nH	0402	SPDT RF blocking for biasing	Würth Elektronik, WE-MK	74478422	WE
L2	~~4.7nH~~ (shorted)	0402	LNAout matching	Würth Elektronik, WE-MK	744784047	WE
L3	18nH	0402	PAout Matching	Würth Elektronik, WE-MK	74478418	WE
L4	2.7nH	0402	LNA input match	Würth Elektronik, WE-MK	744784022	WE
L5	6.8nH	0402	Optional optimising of the PA input	Würth Elektronik, WE-MK	744784068	WE

Part Number	Value	Size	Function / short explanation	Manufacturer	Order Code	Order source
C1	1nF	0402	medium RF short for SPDT bias	Murata, X7R	GRP155R71H102KA01B	Murata
C2	6.8pF	0402	medium RF short for SPDT bias	Murata, C0G	GRP1555C1H6R8DZ01B	Murata
C3	6.8pF	0402	Antenna DC decoupling	Murata, C0G	GRP1555C1H6R8DZ01B	Murata
C4	2.2pF	0402	RF short SPDT shunt PIN	Murata, C0G	GRP1555C1H2R2CZ01B	Murata
C5	4.7pF	0402	DC decoupling LNA input + match	Murata, C0G	GRP1555C1H4R7CZ01B	Murata
C6	4.7pF	0402	RF short output match	Murata, C0G	GRP1555C1H4R7CZ01B	Murata
C7	1pF	0402	LNA output matching	Murata, C0G	GRP1555C1H1RCZ01B	Murata
C8	10uF/10V	A	Removes the line ripple together with R8-R14	Epcos, HighCap B45196H2106+10 *	25D1820	Bürklin
C9	100nF	0603	Ripple rejection PA	no name	internal stock	Bürklin
C10	47pF	0402	DC decoupling PA input	Murata, C0G	GRP1555C1H470JZ01B	Murata
C11	22pF	0402	RF short-bias PA	AVX, 1B/C0G/NP0	04025A220JAT2A	AVX
C12	1nF	0402	RF short-bias	Murata, X7R	GRP155R71H102KA01B	Murata
~~C13~~	~~2.2uF/16V~~ optional	A	~~RF short; not used because switch on of PA will be delayed but don't removes line ripple; maybe optional for ext. Vcc~~	Epcos, Tantal SMD Standard; B45196E2225K109	25D1020 internal stock	Bürklin
C14	2.2pF	0402	TX-PAout DC decoupling + matching	Murata, C0G	GRP1555C1H2R2CZ01B	Murata
C15	10u/10V	A	dc rail LNVcc	Epcos, HighCap B45196H2106+10 *	25D1820	Bürklin
C16	1.2nF	0603	dc noise LNctrl	no name	internal stock	Bürklin
C17	2.2uF/10V	A	dc rail	Epcos, Tantal SMD Standard; B45196E2225K109	25D1020	Bürklin
C18	1.2nF	0603	dc noise SPDT	no name	internal stock	Bürklin
C19	1.2nF	0603	dc noise PActrl	no name	internal stock	Bürklin
C20	1.2nF	0603	dc noise LNVcc	no name	internal stock	Bürklin
C21	4.7pF	0402	RF short for optional LNA input match	Murata, C0G	GRP1555C1H4R7CZ01B	Murata
PCB	FR4 compatible	45mm X 40mm	Epoxy 560µm; Cu=17.5µm; Ni=5µm; Au=0.3µm two layer double side	www.isola.de Häfele Leiterplattentechnik	DURAVER®-E-Cu, Qualität 104 ML B-DE 104 ML/2	Häfele
X1	SMA, female pin	Microstrip	Antenna connector	Huber+Suhner, panel launcher, female, tab contact	23 SMA-50-0-2/111 NE	Suhner
X2	SMA, female pin	Microstrip	RX-Out connector	Huber+Suhner, panel launcher, female, tab contact	23 SMA-50-0-2/111 NE	Suhner
X3	SMA, female pin	Microstrip	TX-IN connector	Huber+Suhner, panel launcher, female, tab contact	23 SMA-50-0-2/111 NE	Suhner

1.2.4. The PCB


BGU2003
BGA6589
BAP51-02
ANT
RX
TX
Philips Semiconductors
European Support Group
2.4GHz Generic Front End


BGU2003
BGA6589
BAP51-02
GND
RX
ANT
TX
SPDT
Philips Semiconductors
European Support Group
2.4GHz Generic Front End

1.2.5.Functional description

1.2.5.1. Principle of operation

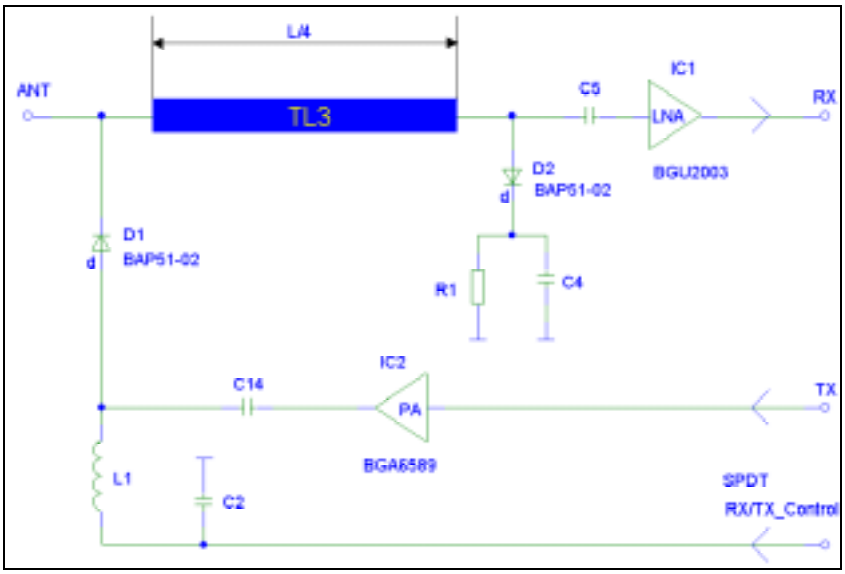


Figure 30: Principle working of the SPDT for multiplexing PA and LNA

A dc voltage on RX/TX Control terminal passes L1 and forward biases the PIN diodes D1 and D2. The dc current is adjusted by R1. Because of the principle function of a PIN diode, D1 and D2, have a very low resistance R_{ON}. This can be assumed as a RF short. Due to this, the input of the LNA input is connected via D2 and the capacitor C4 to GND. C5 prevents any change of DC potential at the LNA input. For the principle function it can be assumed as a short for RF signals. The result is a very low volume of ANT-Signals amplified by IC1. From the power ratio RX/ANT is calculated the ***RX-ANT isolation*** for switched on transmitter. C14 prevents any dc level change on the PA output.

The 50Ω Microstrip (µStrip) transmission line TL3 mechanical dimension is designed to be a symmetrical quarter wave length transformer. That means its electrical length is $= \frac{\lambda}{4}$.

With λ=wave-length inside the used µStrip substrate. As explained in the RF-Design-Basics chapter the L/4 line do transform impedance: $Z_{OUT} = \frac{Z_L^{\ 2}}{Z_{IN}}$

A short on one side causes the L/4 -transformer an transformation into an open appearing on the other µStrip side. The mathematical issue is shown side by. Due to this action the LNA input is shorted to GND but on the other side appears the RX-rail as an open on the ANT-terminal. That means the RX-rail is switched out of the circuit. Due to the very low resistant D1 the output power of the PA are transferred with very low losses to the ANT-terminal. The power ratio of ANT/PA-out is the switch ***TX-insertion loss***. The rest of TX signals appearing at the RX output are defined by the power ratio RX/TX called ***RX/TX coupling.***

Microstrip L/4 transformer analysis:

Transmission-Line ***(TL)***: $\underline{Z_1} = Z_L \frac{\frac{Z_2}{Z_L} + j\tan\beta\cdot}{1 + j\frac{Z_2}{Z_L}\tan\beta\cdot}$

$$\underline{Z_1} = Z_L \frac{\frac{Z_2}{Z_L} + j\tan\left(2\pi\frac{}{\lambda}\right)}{1 + j\frac{Z_2}{Z_L}\tan\left(2\pi\frac{}{\lambda}\right)} = Z_L \frac{x + j\tan\left(2\pi\frac{}{\lambda}\right)}{1 + jx\tan\left(2\pi\frac{}{\lambda}\right)}$$

with $= \frac{\lambda}{4}$ causes $\underline{Z_1} = Z_L \frac{x + j\tan\left(\frac{\pi}{2}\right)}{1 + jx\tan\left(\frac{\pi}{2}\right)}$

$\tan\left(\frac{\pi}{2}\right) = \infty$ non defined ratio $\frac{\infty}{\infty}$ by lim analysis

cont. next page…

Removal of the RX/TX_Control dc voltage put the PIN-diodes in the off state. In this sate they are highly resistive with a very low parallel capacity. This is another very important characteristic of PIN diodes. In this bias status the output power of IC2 are blocked by D1 and cant reach the ANT-terminal ***(TX-PA isolation or TX leakage)***. Because D2 is very high resistive the µStrip do only see the LNA's input impedance of 50Ω. As illustrate by the L/4 mathematical function, the µStrip output impedance will be 50Ω too. Due to it, the ANT-signals are low loss transferred to the LNA and appears low noise amplified on the RX output terminal.
The diodes D1 and D2 do form a switch with one common PIN and two independent pins. This is called a single pole double trough switch ***(SPDT)***.

$$\underline{Z_1} = Z_L \frac{x + jy}{1 + jxy} = Z_L \frac{\frac{x}{y} + j}{\frac{1}{y} + jx}$$

$$\lim_{y \to \infty} \left(\underline{Z_1}\right) = Z_L \frac{0 + j}{0 + jx} = Z_L \cdot \frac{j}{jx}$$

$$\underline{Z_1} = Z_L \cdot \frac{Z_L}{\underline{Z_2}} \qquad \boxed{\underline{Z_1} = \frac{Z_L^2}{\underline{Z_2}}}$$

Special cases:

open	short;	C	L
short	open;	L	C

1.2.5.2. Circuit Details

- ***PLEASE NOTE: - DC SUPPLY SETUP -***

For protecting the demoboard against over voltage and wrong polarity during bench experiments, the main board connectors do have an input shunt Z-Diode {D7, D8, D9}. In a bias fault conditions they shunt the terminals to GND. Due to this, please adjust the current limiter of your dc power supply and check proper polarity and right amount of voltage. Several LEDs on the board monitors the main board functions for visual feedback to the hardware/software user.

- ***SPDT:***

The SPDT is build by the circuit {D1, D2, R1, C4, C3, L1, C2, C1}. It function is controlled by the circuit Q3, D6, R6, R7, C18. The PIN diode forward current is set-up by R1. C4 do short the cathode of D2 to GND. C3 couple the Antenna to the switch by removal of dc components. L1 is high resistive for the RF but do pass the dc current into the diodes. C2, C1 do short remaining rests of RF. AT Checkpoint T3, the dc voltage across the SPDT switch can be measured. The combination of D6, D5 and B-E of Q3 forms a level shifter for proper switching of Q3 by a 3V logic signal. R6 makes sure defined operation of D6. A lighting D5 caused by SPDT=LOW do illustrated a switch mode of connecting the antenna terminal to the PA output. C18 removals coupled in line noise cause by long wires connected to the board. C5 and C14 prevent a dc rail into the MMICs. The principle SPDT function based on the quarter wavelength µStrip line TL3 is explained in the former chapter.

- ***LNA:***

The LNA (IC1) supply bias is comparable to a pull up circuit for an open collector. The LNA supply voltage is connected to terminal LNVcc. C20 and C15 removals switching peaks, coupled-in noise and line growl. D9 do limit the voltage to abs. max. =3.6V. Input voltage of > 3.6V will source down the current limiter of the lab power supply for over voltage protection and wrong polarity of the LNA circuit. R4 do set up the bias operation point of the LNA output circuit. C6 defines a clear short to GND for the L2. L2-C7 combination forms an output matching circuit for the LNA. Additionally L2 do pass the dc supply into the MMIC PIN4. The optional R3 can be used for making more broadband the output circuit or for damping of oscillation. The operation and gain adjust is done by a current into the control PIN3. The control current is adjusted and limited by R2. C16 acts for wire noise reduction. D8 protects again over voltage (>3.6V) and wrong polarity.

With LNctrl=HIGH, the LNA is switched on with max. Gain. This is illustrated by lighting D3. LNctrl voltages between 0V and 3.0V can be used for standby, max. Gain and variable gain like AGC. The voltage potential difference between LNctrl and test point T5 (across R2) can be used for calculating the actual control current into PIN3. Depending on the amount of R12 the LED. D3 do illustrate the actual LNA-Gain. Because the LNA input impedance and noise optimum impedance are closed to 50Ω there is no further need of input matching circuit. C5 do removal dc components. If there is the need for further experimental input matching experiments, the combination of C5 and the optional L4-C21 can be used by the customer.

PA:

The power amplifier MMIC (IC2) does it self need a supply of ca. 4.7V/83mA sinking into the output PIN3. For temperature stabilisation of the output voltage-current temperature relationship, there is the need of series resistors {R8, R13, R14}. L3 do inject the dc supply current into the MMIC. Additionally L3 blocks the RF. RF leakage behind it is shunt to GND by C11. C12 do back up for medium frequencies and ripples caused by e.g. large output envelope change. At test point T2 can be monitored the PA output dc voltage. By the use of {Q1, R10, C19} the PA can be switched off. For an open terminal PActrl, R9 makes sure of full conducting Q1. D4 do light for switched on power amplifier. The optional L5 can be used for input matching optimisation experiments. D7 do protect the PA against over voltage on wrong polarity.

1.3. Data Sheet "2.4GHz Generic Front-End"

Philips Semiconductors European Support Group

Objective specification
2003 May 15

2.4GHz Generic Front-End Demoboard

BGA6589, BGU2003, BAP51-02

FEATURES

- 2.4GHz ISM band operation
- 50Ω female SMA connectors
- LNA, PA and SPDT on board
- Supply control function
- LED's indicates the operation mode

APPLICATIONS

- Bluetooth
- W-LAN
- ISM
- Home video and TV link
- Remote control

DESCRIPTION

The demoboard is intended to be used as a generic Front-End Module in front of a high integrated half duplex IC chip set. It uses an LNA-MMIC (BGU2003) for improving the receiver Sensitivity and a PA-MMIC (BGA6589) for increasing the transmitter distance. A controlled SPDT based on PIN-Diodes (BAP51-02) switch the LNA or the PA to the common antenna terminal e.g. a 50Ω ceramic patch antenna can be connected.

PINNING

PIN / PORT	DESKRIPTION
ANT	Bi-directional Antenna I/O
GND	Ground
LNctrl	LNA control
LNVcc	LNA dc supply
RX	LNA 50Ω out
SPDT	SPDT control RX/TX
PAVcc	PA dc supply
PActrl	PA control
TX	PA control

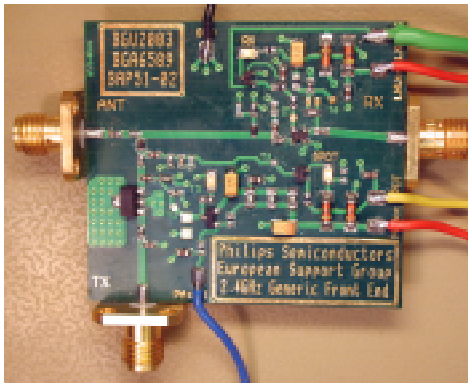


Fig.1 Demoboard Top View

Note:

1. USL=Upper Spec Limit; LSL=Lower Spec Limit
2. USL and LSL are calculated according Philips' 6-Sigma Statistic Process Control (SPC) definition for Cp=2.0
3. MIN and MAX data are determined by the max. spread measured on 10 investigated demoboards

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
BW	bandwidth		2401		2498.5	MHz
PAVcc	DC supply voltage	PA		9		V
LNVcc	DC supply voltage	LNA		3		V
$I_{(PAVcc)}$	supply current	PA				mA
$I_{(LNVcc)}$		LNA				mA
$I_{(stby)}$	standby supply current	I (PAVcc)+ I(LNVcc)				µA
S_{21}	forward power gain	LNA receive (RX)				dB
		PA transmit (TX)				dB
NF	noise figure	2450MHz, LNA		tbf		dB
$P_{L\ 1dB}$	load power at 1dB gain compression	LNA output; 2450MHz		+9.1		dBm
		PA output; 2450MHz		+16.9		dBm

LIMITING VALUES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
PAVcc	DC supply voltage	PA; note 1	0	9	10	V
LNVcc	DC supply voltage	LNA; note 1	0	3	3.6	V
SPDT	SPDT switch control		0	0/3/5	PAVcc	V
LNctrl	LNA power control	note 1	0	0/3	3.6	V
PActrl	PA power control		0	0/9	PAVcc	V

Note:

1. The board is protected by a Z-Diode to GND. Negative voltages or voltage at the limit do cause this diode to shunt a large current to GND. This is for protecting the board against wrong polarity and over voltage during bench experiments.

ACTIVE DEVICES THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS		VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to solder point	BGA6589, $T_S \leq 70$ °C; note 1		100	K/W
		BGU2003		85	
		BAP51-02		350	
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	BC847BW; note 2		625	
		BC857BW; note 3		625	
		PBSS5140T	in free air; note 4	417	
			in free air; note 5	278	

Note:

1. T_S is the temperature at the soldering point of pin 4.
2. Transistor mounted on an FR4 printed-circuit board.
3. Refer to SOT323 standard mounting conditions.
4. Device mounted on a printed-circuit board, single sided copper, tinplated and standard footprint.
5. Device mounted on a printed-circuit board, single sided copper, tinplated and mounting pad for collector 1cm^2.

CHARACTERISTICS DATA DEFINITION

The MIN. and MAX. data are the data spread measured on 10 investigated demo boards versus different conditions. This caused the measurement of 1540 data points. The TYP. data is arithmetic average of the measurement done on 10 demo boards (=mean of an assumed symmetrical Gaussian process spread). The process spec limits LSL and USL are calculated on Philips 6-Sigma SPC statistical process control definition. For details refer to the detailed explained in the application chapter.

STATIC CHARACTERISTICS

PAVcc=9V; LNVcc=3V; Tj=room temperature; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	LSL	MIN.	TYP.	MAX.	USL	UNIT
$I_{(LNVcc)}$	supply current LNA	LNctrl=0V	0.23	0.85	1.096	1.31	1.96	mA
		LNctrl=3V	11.09	14.21	16.03	16.95	20.97	mA
$I_{(PAVcc)}$	supply current PA off	SPDT=5V; PActrl=9V	0	0.2	0.66	1.1	3.19	µA
		SPDT=3V; PActrl=9V	18.43	55.1	63.8	76.1	109.17	µA
		SPDT=0,5V; PActrl=9V	2.69	3.08	3.18	3.34	3.67	mA
		SPDT=0V; PActrl=9V	2.74	3.15	3.25	3.42	3.77	mA
	supply current PA on	SPDT=5V; PActrl=0V	74.72	81.6	83.96	86.5	93.2	mA

CHARACTERISTICS: Return Loss of the Transmitter

PAVcc=9V; LNVcc=3V; RX=50Ω matched; LNctrl=3V; Tj=room temperature; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS		LSL	MIN.	TYP.	MAX.	USL	UNIT
$RL_{IN\ TX}$	return loss input TX; PA=off	SPDT=0V PActrl=9V SPDT=TX	2401MHz	4.76	3.85	3.37	3.05	1.97	dB
			2449.75MHz	4.46	3.54	3.29	2.96	2.12	
			2498.5MHz	4.41	3.51	3.29	2.95	2.17	
	return loss input TX; PA=on	SPDT=0V PActrl=0V SPDT=TX	2401MHz	14.21	11.8	11.08	10.02	7.96	dB
			2449.75MHz	13.4	11.42	10.68	9.87	7.97	
			2498.5MHz	12.83	11.11	10.28	9.57	7.73	
		SPDT=5V PActrl=0V SPDT=RX!	2401MHz	19.95	12.96	9.91	7.7	>0	dB
			2449.75MHz	18.43	12.1	9.44	7.42	0.46	
			2498.5MHz	17.03	11.44	9.02	7.3	1.01	
$RL_{OUT\ ANT}$	return loss output ANT; PA=on	SPDT=0V PActrl=9V SPDT=TX	2401MHz	17.03	12.15	7.32	6.43	2.39	dB
			2449.75MHz	8.72	7.35	7.13	6.56	5.53	
			2498.5MHz	9.24	7.83	7.55	6.98	5.86	
	return loss output ANT; PA=off	SPDT=0V PActrl=0V SPDT=TX	2401MHz	15.24	12.47	11.85	10.81	8.45	dB
			2449.75MHz	16.55	13.27	12.46	11.51	8.38	
			2498.5MHz	18.48	14.3	13.43	11.87	8.38	
		SPDT=1V PActrl=0V SPDT~TX	2401MHz	15.32	12.56	11.87	10.87	8.42	dB
			2449.75MHz	16.57	13.27	12.48	11.5	8.4	
			2498.5MHz	19.11	15.07	13.47	11.92	7.83	

CHARACTERISTICS: Return Loss of the Receiver

PAVcc=9V; LNVcc=3V; RX=50Ω matched; LNctrl=3V; Tj=room temperature; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS		LSL	MIN.	TYP.	MAX.	USL	UNIT
$RL_{IN\ ANT}$	return loss input ANT; PA=off	SPDT=3V LNctrl=3V PActrl=9V	2401MHz	23.55	18.14	16.43	14.2	9.31	dB
			2449.75MHz	25.51	19.01	15.65	12.74	5.79	
			2498.5MHz	20.85	15.75	14.31	12	7.8	
	return loss input ANT; PA=on	SPDT=0V LNctrl=0V PActrl=0V	2401MHz	15.29	12.31	11.21	10.15	7.14	dB
			2449.75MHz	16.61	13.09	11.87	10.66	7.13	
			2498.5MHz	17.69	13.83	12.59	11.32	7.5	
		SPDT=3V LNctrl=3V PActrl=0V	2401MHz	23.93	18.35	16.64	14.28	9.34	dB
			2449.75MHz	22.92	16.99	15.55	12.92	8.18	
			2498.5MHz	21.38	15.95	14.53	12.1	7.67	
$RL_{OUT\ RX}$	return loss output RX; PA=off	SPDT=3V LNctrl=3V PActrl=9V	2401MHz	23.03	18	14.84	13.49	6.64	dB
			2449.75MHz	28.01	19.61	17.77	13.74	7.53	
			2498.5MHz	32.59	20.86	17.69	11.41	2.79	
	return loss output RX; PA=on	SPDT=0V LNctrl=0V PActrl=0V	2401MHz	14.8	9.73	4.72	3.8	5.36	dB
			2449.75MHz	11.13	7.74	4.45	3.79	2.23	
			2498.5MHz	8.87	6.41	4.06	3.52	>0	
		SPDT=3V LNctrl=3V PActrl=0V	2401MHz	22.84	17.9	14.93	13.64	7.01	dB
			2449.75MHz	28.4	19.78	17.95	13.8	7.5	
			2498.5MHz	32.88	21.02	17.83	11.5	2.78	

CHARACTERISTICS: RX and TX gain

PAVcc=9V; LNVcc=3V; Tj=room temperature; unless otherwise specified
S21(TX): NWA Port1-IN TX; NWA Port2-ANT;RX=50Ω matched
S21 (TX/RX): NWA Port1-IN TX; Port2-Out RX; ANT=50Ω
S12 (TX) : NWA Port1-IN TX; NWA Port2-ANT;RX=50Ω matched

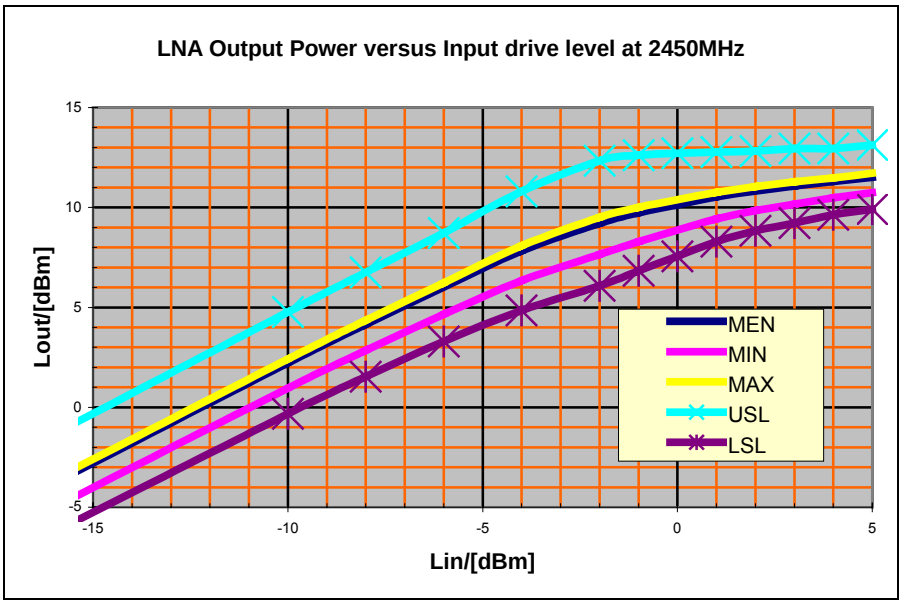
SYMBOL	PARAMETER	CONDITIONS		LSL	MIN.	TYP.	MAX.	USL	UNIT
S21 (TX)	forward gain PA PA=on	SPDT=0V LNctrl=0V PActrl=0V	2401MHz	13.95	14.75	14.98	15.33	16.02	dB
			2449.75MHz	13.89	14.63	14.87	15.2	15.85	
			2498.5MHz	13.72	14.46	14.71	15.04	15.71	
		SPDT=0V LNctrl=0V PActrl=3V	2401MHz	13.96	14.76	15	15.34	16.03	dB
			2449.75MHz	13.88	14.65	14.89	15.23	15.9	
			2498.5MHz	13.76	14.5	14.75	15.07	15.73	
S12 (TX)	reverse gain PA PA=on	SPDT=0V LNctrl=0V PActrl=0V	2401MHz	25.44	24.66	24.27	24	23.09	dB
			2449.75MHz	25.22	24.5	24.09	23.8	22.96	
			2498.5MHz	25.08	24.29	23.93	23.6	22.78	
S21 (RX)	forward gain LNA PA=off	SPDT=3V LNctrl=9V PActrl=3V	2401MHz	11.21	12.2	13.17	13.4	15.12	dB
			2449.75MHz	10.69	11.87	13.03	13.24	15.37	
			2498.5MHz	10.08	11.43	12.77	12.96	15.46	
	forward gain LNA PA=on	SPDT=3V LNctrl=0V PActrl=3V	2401MHz	11.1	12.13	13.13	13.35	15.15	dB
			2449.75MHz	10.66	11.83	12.98	13.19	15.3	
			2498.5MHz	10.06	11.39	12.72	12.92	15.37	
S12 (RX)	reverse gain PA PA=on	SPDT=3V LNctrl=9V PActrl=3V	2401MHz	18.79	18.1	17.91	17.58	17.04	dB
			2449.75MHz	18.29	17.8	17.62	17.45	16.96	
			2498.5MHz	18.05	17.67	17.48	17.36	16.92	
S21 (TX/RX)	coupling TX RX PA=LNA=on	SPDT=3V LNctrl=0V PActrl=3V	2401MHz	6.45	8.37	9.36	10.21	12.28	dB
			2449.75MHz	6.22	8.16	9.36	10.2	12.5	
			2498.5MHz	5.86	7.88	9.24	10.09	12.61	

CHARACTERISTICS: LNA out of band gain

For characterisation the sensitivity against received signals out side the 2.4GHz ISM band.

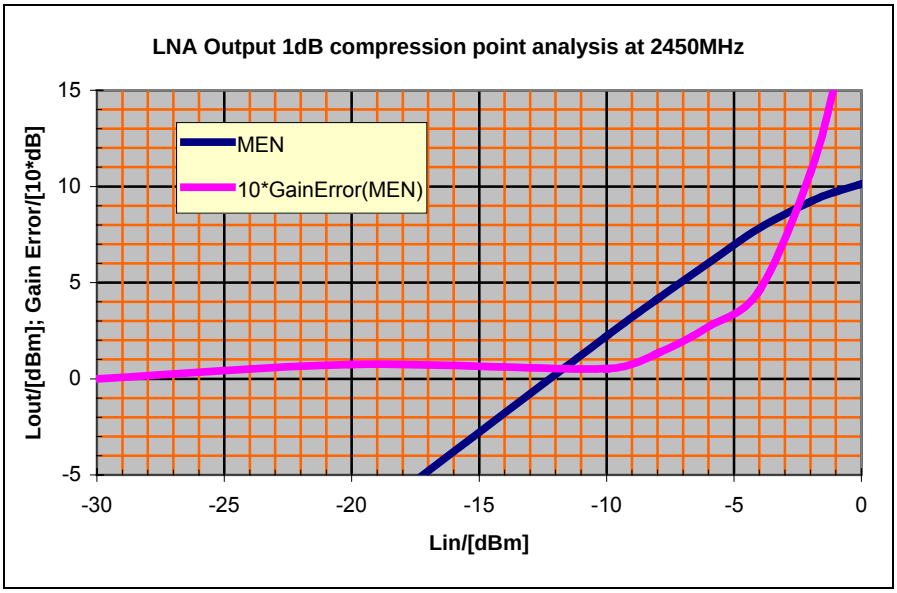
PAVcc=9V; LNVcc=3V; PActrl=9V; TX=50Ω matched; Tj=room temperature; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	LSL	MIN.	TYP.	MAX.	USL	UNIT
S21 (RX)	forward gain LNA	148.71MHz	-14.58	-13.56	-13.21	-12.76	-11.83	dB
		314.5MHz	-9.57	-7.69	-7.28	-6.28	-5	
		431.5MHZ	-8.31	-6.53	-6.04	-5.08	-3.77	
		899.5MHz	-14.96	-13.07	-12.45	-11.87	-9.93	
		1903.75MHz	-0.32	2.6	3.7	4.75	7.72	
		2449.75MHz	10.66	11.86	13.05	13.24	15.44	
		3600.25MHz	4.19	5.69	6.7	7.24	9.21	
		4000MHz	3.81	4.91	5.6	6.03	7.38	



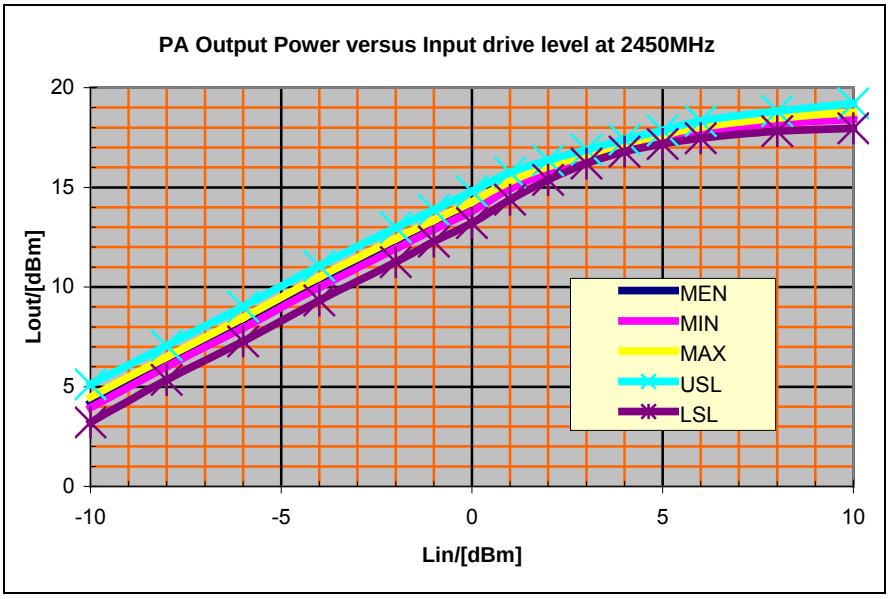
LNA-PL$_{1dB}$ set-up:

LNVcc=3V
PAVcc=9V
SPDT=LNctrl=3V;
PActrl=9V
ANT=hp8594E with 40dB attenuator fixed setting
TX=SME03
RX=50Ω match



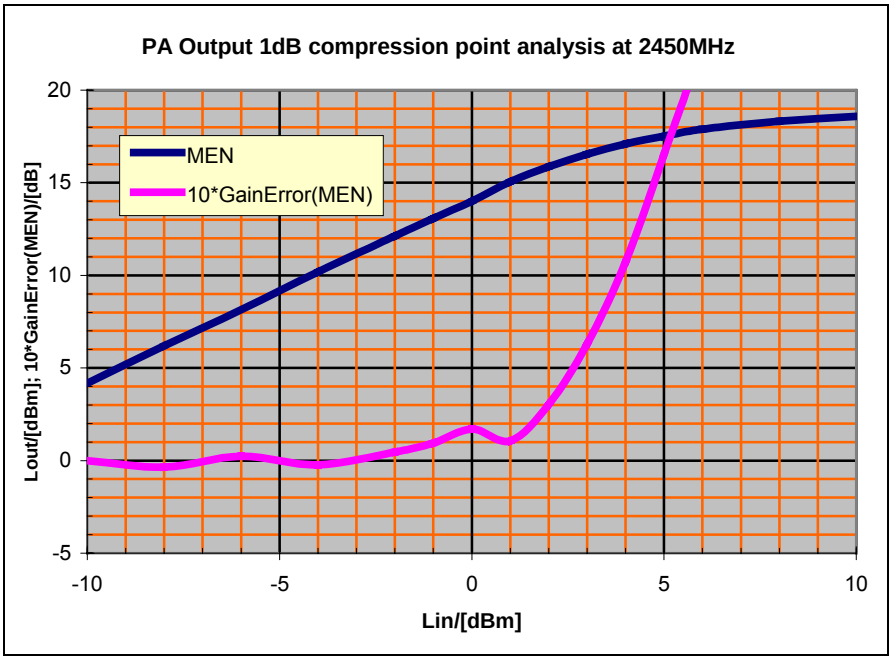
The 1dB compression point is found at a gain error of 1dB

LNA 1dB compression point of the LNA at 2450MHz:
PL$_{1dB(IN)}$≈-2,2dBm
PL$_{1dB(OUT)}$≈+9,1dBm
This is an arithmetic average value (TYP.)



LNA-PL_{1dB} Setup:

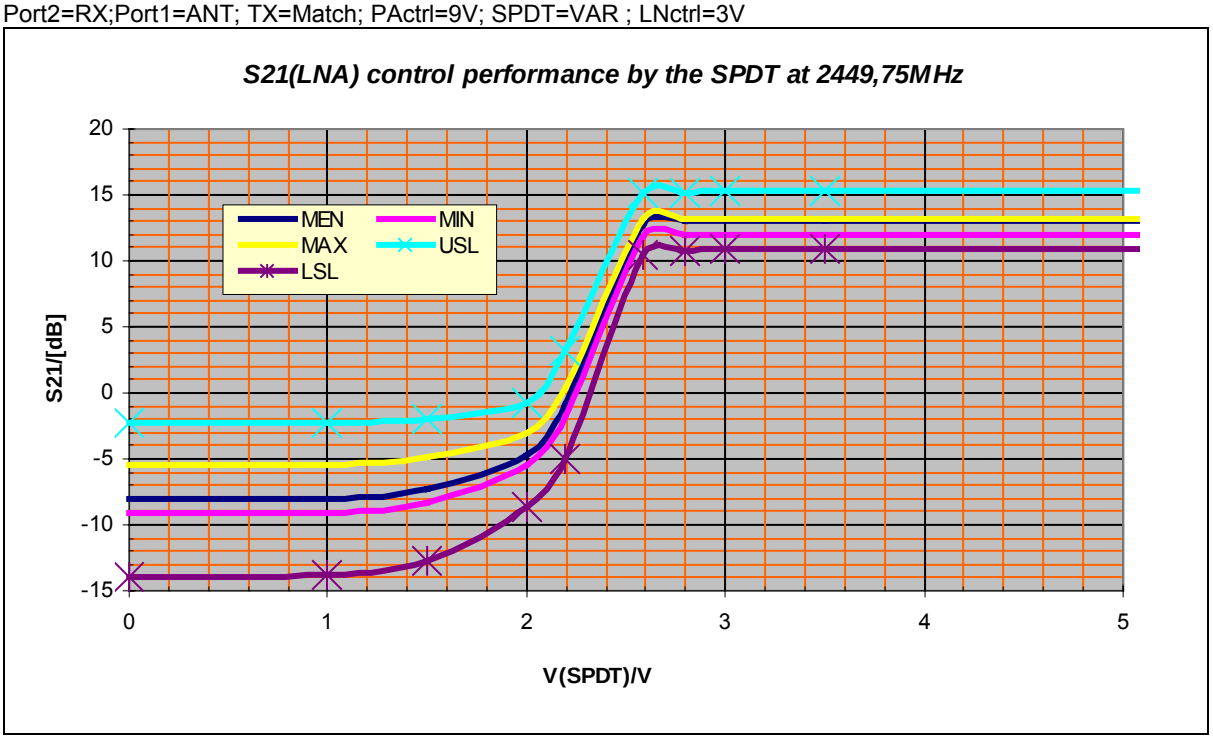
LNVcc=3V
PAVcc=9V
SPDT=LNctrl=3V;
PActrl=9V
ANT=hp8594E with 40dB attenuator fixed setting
TX=SME03
RX=50Ω match



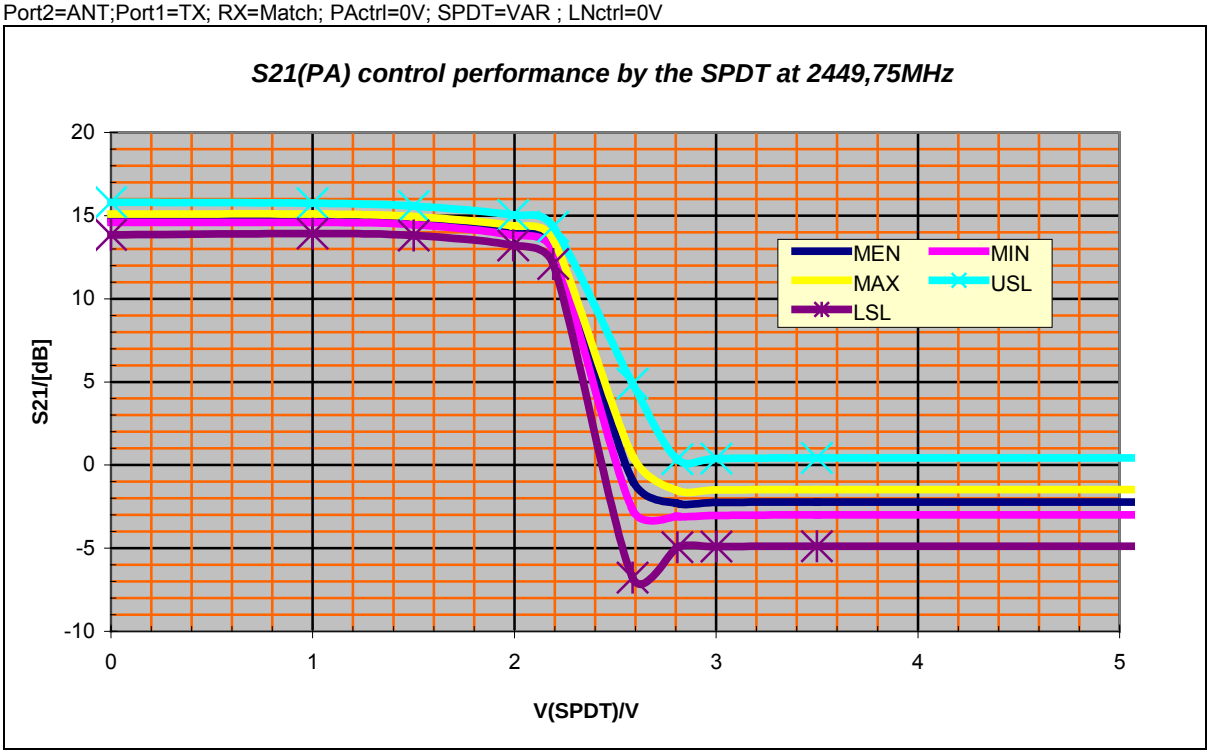
PA 1dB compression point of the LNA at 2450MHz:
$PL_{1dB(IN)}$≈+3,8dBm
$PL_{1dB(OUT)}$≈+16,9dBm
This is an arithmetic average value (TYP.)

The 1dB compression point is found at a gain error of 1dB

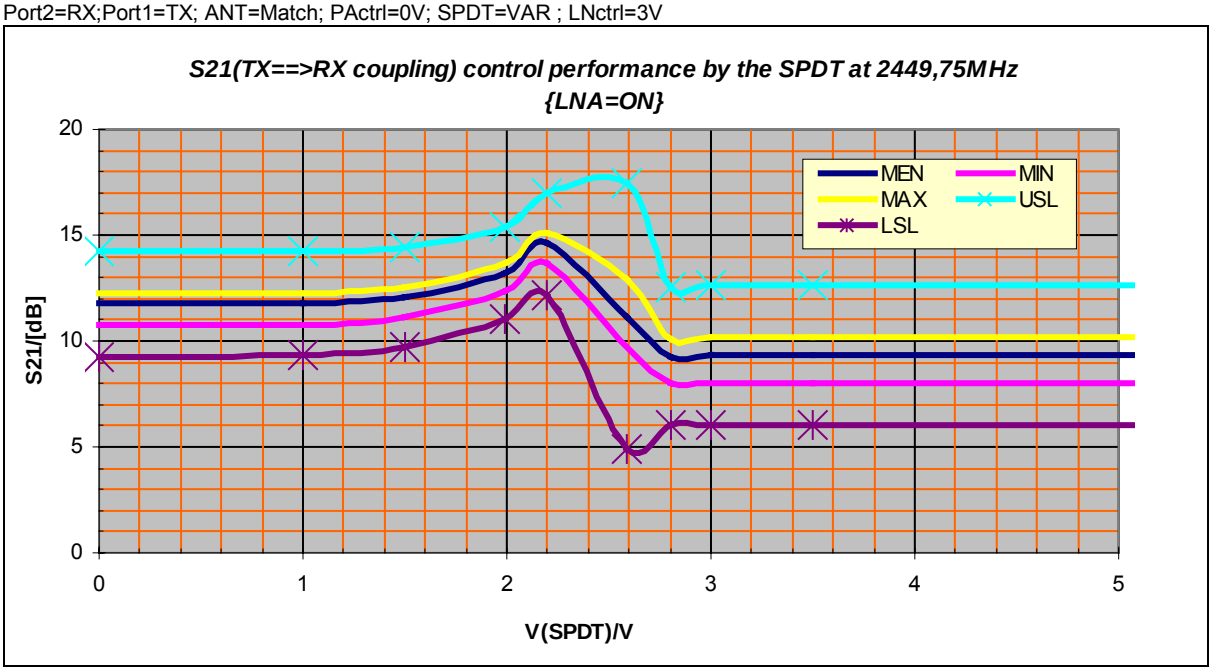
Port2=RX;Port1=ANT; TX=Match; PActrl=9V; SPDT=VAR ; LNctrl=3V



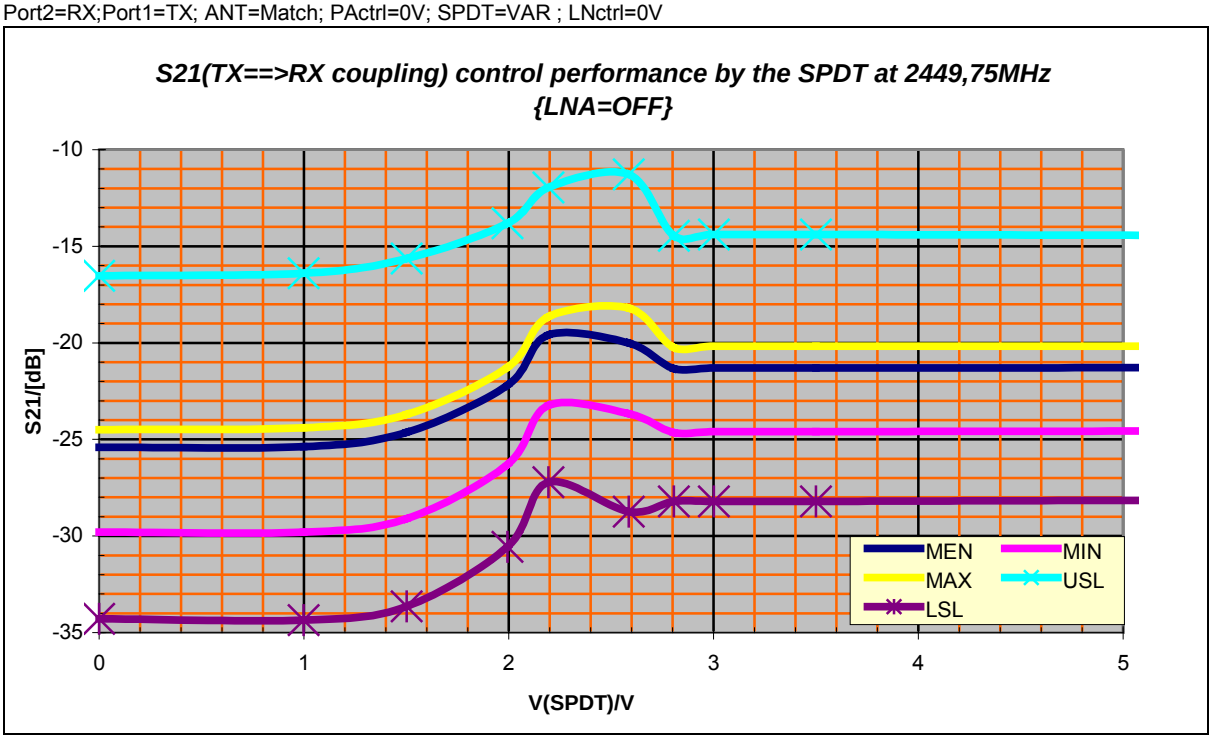
Port2=ANT;Port1=TX; RX=Match; PActrl=0V; SPDT=VAR ; LNctrl=0V



Port2=RX;Port1=TX; ANT=Match; PActrl=0V; SPDT=VAR ; LNctrl=3V



Port2=RX;Port1=TX; ANT=Match; PActrl=0V; SPDT=VAR ; LNctrl=0V



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Author:
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RF Discretes Small Signal Application Engineer

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Appendix B: Application note

BB202, low voltage FM stereo radio (TEA5767/68)

Author(s): M Ait Moulay , Philips Semiconductors Strategic Partnership Catena

The Netherlands, Date: 18-06-2002

This is a shortened application note to emphasise the BB202 varicap as an important FM oscillator next to the TEA5767/68 single chip stereo FM receiver (complete application note: AN10133).

Summary

The TEA5767/68 is a single-chip stereo FM receiver. This new generation, low-voltage FM radio has a fully integrated IF with selectivity and demodulation. The IC does not require any alignment, which eliminates bulky and expensive external components.

The digital tuning approach is based on conventional PLL concepts. With software, the radio can be tuned into the European, Japanese, or US FM bands.

The power consumption for the tuner is low. Supply current is about 13 mA and supply voltage can be varied between 2.5 and 5V.

The radio finds applications in many areas, especially in portable applications such as mobile phones and portable CD and MP3 players.

This application note describes this FM radio in a small size and low voltage application. To demonstrate the operation of the tuners a demonstration board is developed, which can be extended with a software controllable amplifier and a RDS chip. The complete application can be controlled from a PC by means of demonstration software.

Introduction

Consumer demand for more integrated and low power IC's has increased tremendously in the last decade. The IC's must be smaller, cheaper and consume less power. This is especially true for portable equipment like mobile phone, CD, MP3 and cassette players, where battery life and a large feature set is very important. To integrate an FM radio in this kind of equipment it is important that the radio function be small and the overall power consumption of the radio function is low. The **TEA5767/68** is a single chip, digitally tuned FM stereo radio. The device is small, has a very low current consumption and is completely adjustment free. This simplifies the PCB design and saves design-in time. The tuner contains all the blocks necessary to build a complete digitally tuned radio function.

The FM tuners consist of three IC's in 32 pins or 40 pins package. These IC's can be controlled via either a 3-Wire or an I^2C (or both) bus interface.
A small PCB demonstration board has been designed on which any of the three IC's can be mounted. These demo boards can be placed on a motherboard, which can be extended with an audio amplifier and a **R**adio **D**ata **S**ystem (**RDS/RBDS)** IC.

The three tuners are:

- TEA5767HN FM stereo radio, 40 leads with I²C and 3-Wire bus interface, Body 6*6*0.85 mm, SOT1618
- TEA5767HL FM stereo radio, 32 leads with 3-Wire bus interface, Body: 7*7*1.4 mm, SOT358.
- TEA5768HL FM stereo radio, 32 leads with I²C bus interface, Body: 7*7*1.4 mm, SOT358.

In this application note only one IC, the TEA5767HN, and one demonstration board will be described. However, this description can be applied to the other boards.

1. The TEA5767

A block diagram of the TEA5767HN is given in Figure 1. The block diagram consists of a number of blocks that will be described according to the signal path from the antenna to the audio output.

The RF antenna signal is injected into a balanced low noise amplifier (LNA) via a RF matching circuit. In order not to overload the LNA and the mixer the LNA output signal is fed to an automatic gain control circuit (AGC). In a quadrature mixer the RF signal is converted down to an IF signal of 225KHz by multiplying it with a local oscillator signal (LO). The chosen mixer architecture provides inherent image rejection.
The VCO generates a signal with double the frequency necessary for the I/Q mixer structure. In the N1 divider block, the required LO signal is created. The frequency of the VCO is controlled with a PLL synthesiser system.
The I/Q signals out the mixer are fed to an integrated IF filter (RESAMP block). The IF frequency of this filter is controlled by the IF Centre Frequency adjust block.
The IF signal is then passed to the limiter block, which removes the amplitude variation from the signal. The limiter is connected to the level ADC and the IF counter blocks. These two blocks provide the proper information about the amplitude and frequency of the RF input signal, which will be used by the PLL as stop criterion.
The IC has a quadrature demodulator with an integrated resonator. The demodulator is fully integrated which makes IF alignments or an external resonator unnecessary.

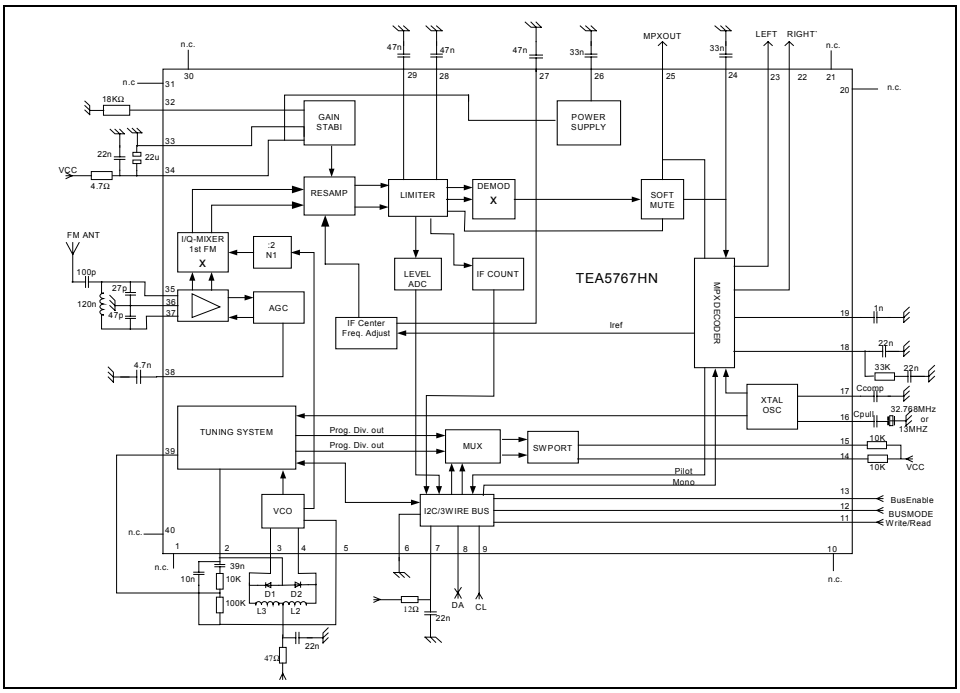

Figure 1 Block application diagram of the TEA5767HN

The **stereo decoder (MPX decoder)** in its turn is adjustment free and can be put in mono mode from the bus interface. The stereo noise cancelling (SNC) function gradually turns the stereo decoder from 'full stereo' to mono under weak signal conditions. This function is very useful for portable equipment since it improves the audio perception quality under weak signal conditions.

The "soft-mute" function suppresses the inter-station noise and prevents excessive noise from being heard when the signal level drops to a low level.

The tuning system is based on a conventional PLL technique. This is a simple method in which the phase and the frequency of the VCO are continuously corrected, with respect to a reference frequency, until frequency acquisition takes place. Communication between the tuning system and an external controller is possible via a 3-Wire or I^2C bus interface.

2 FM STEREO Application

The application is identical for the three IC's as mentioned in chapter 1. This application comprises two major circuits: RF input circuit and a FM oscillator circuit.

The communication with a µ-computer can be performed via an I^2C or a 3-Wire serial interface bus, selectable with BUSMODE pin, for the TEA5767HN. TEA5768HL operates in I^2C bus mode and TEA5757HL in 3-Wire bus mode. The receivers can work with 32.768KHz or 13MHz clock crystal, which can be programmed by the bus interface. The PLL can also be clocked with 6.5MHz clock signal. Three audio outputs are available: audio left, audio right and MPX (multiplex). A basic application diagram of the FM receiver is shown in Figure 2.

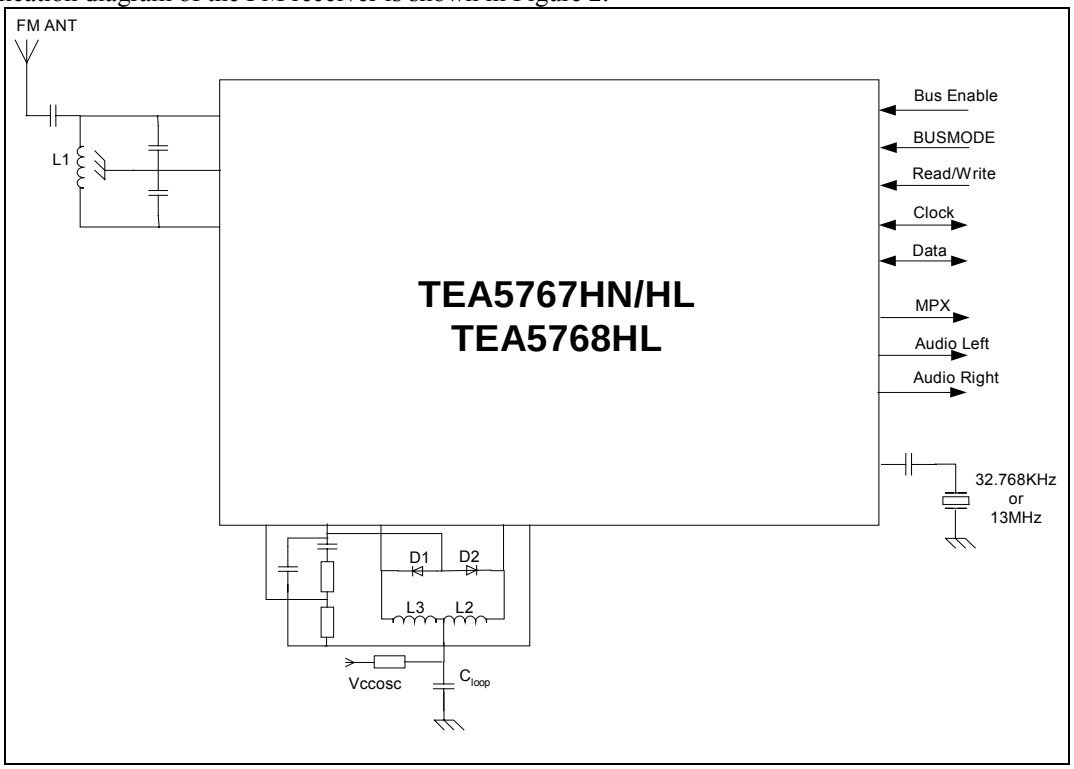

Figure 2 Basic application diagram of TEA5767/68 stereo radio

3 TEA5767HN package

The TEA5767HN FM stereo radio is a 40 pins HVQFN (SOT1618) package IC which can be operate with I^2C or 3-Wire bus interface. The fully integrated IF selectivity and demodulation make it possible to design a very small application board with a minimum of very small and low cost components. The outline of the TEA5767HN package is 6*6*0.85 mm.

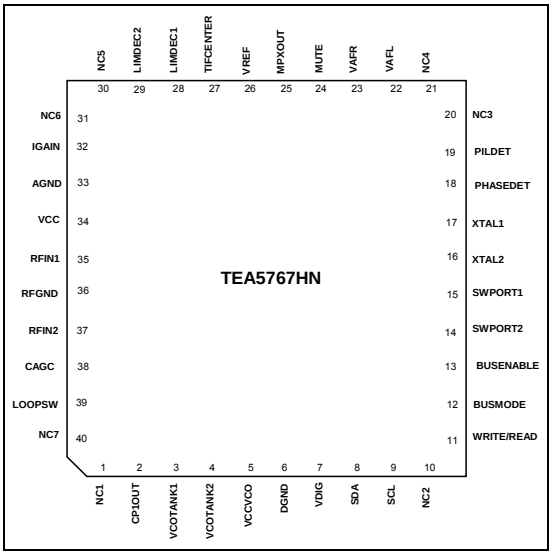

Figure 3 Pinning of the TEA5767HN (HVQFN40)

Figure 3 shows the pinning of the TEA5767HN and Table 1 gives a description of each pin of the IC.

SYMBOL	PIN	DESCRIPTION	Voltage min.	SYMBOL	PIN	DESCRIPTION	Voltage min.
NC1	1	Not connected		NC4	21	Not connected	
CPOUT	2	Charge pump output of the synthesiser PLL	1.64V	VAFL	22	Audio left output	
VCOTANK1	3	VCO tuned circuit output 1	2.5V	VAFR	23	Audio right output	
VCOTANK2	4	VCO tuned circuit output 2	2.5V	TMUTE	24	Time constant for the softmute	1.5V
VCCVCO	5	VCO supply voltage	2.5V	MPXOUT	25	FM demodulator MPX out	
DGND	6	Digital ground	0V	VREF	26	Reference voltage	1.45V
VDIG	7	Digital supply voltage	2.5V	TIFCENTER	27	Time constant for IF centre adjust	1.34V
DATA	8	Bus data line input/output		LIMDEC1	28	Decoupling IF limiter 1	1.86V
CLOCK	9	Bus clock line input		LIMDEC2	29	Decoupling IF limiter 2	1.86V
NC2	10	Not connected		NC5	30	Not connected	
WRITE/READ	11	Write/read control for the 3-Wire bus		NC6	31	Not connected	
BUSMODE	12	Bus mode select input		IGAIN	32	Gain control current for IF filter	0.48V
BUSENABLE	13	Bus enable input		AGND	33	Analog ground	0V
SWPORT1	14	Software programmable port 1		VCC	34	Analog supply voltage	2.5V
SWPORT2	15	Software programmable port 2		RFIN1	35	RF input 1	0.93V
XTAL1	16	Crystal oscillator input 1	1.64V	RFGND	36	RF ground	0V
XTAL2	17	Crystal oscillator input 2	1.64V	RFIN2	37	RF input 2	0.93V
PHASEDET	18	Phase detector loop filter	1.0V	CAGC	38	Time constant RF AGC	
PILDET	19	Pilot detector lowpass filter	0.7V	LOOPSW	39	Switch output of synthesiser PLL filter	
NC3	20	Not connected		NC7	40	Not connected	

Table 1 pinning description of the TEA5767HN

4 VCO tank circuit

The VCO circuit produces a signal at double frequency necessary for the tuning system. A divider will halve the frequency of this signal and then deliver it to the PLL.

In the proposed application the used tuning diodes D1 and D2 are BB202**.** This ultra small diode is fabricated in planar technology. It has a low series resistance (0.35Ω typical), which is very important for the signal to noise ratio (SNR). In Figure 4, the capacitance value of this diode is given as function of the reverse voltage.
In our application proposal these diodes can tune the complete FM band (71-108MHz) with less then 3V-supply voltage. The minimum voltage at pin 34 (V_{CC}) should be 2.5V and the maximum voltage 5V. Inside the IC a charge pump is responsible for delivering the required current to charge/discharge the external loop capacitor. During the first 9 ms the charge pump delivers a fast current of 50uA. After this time, the current is reduced to 1µA.

In the given application the typical tuning voltage is between 0.54V (2*108MHz) and 1.57V (2*87.5MHz).

The minimum voltage to frequency ratio, often referred to VCO conversion factor (K_{vco}), is thus about 40MHz/V. The oscillator circuit is designed such that the tuning voltage is between **0.2V and V_{cc}-0.2V**. In order to match the VCO tuning range two serial coils L2 and L3 are put in parallel with the tuning diodes D1 and D2. A typical FM oscillator-tuning curve, using BB202 tuning diodes, is given in Figure 5.
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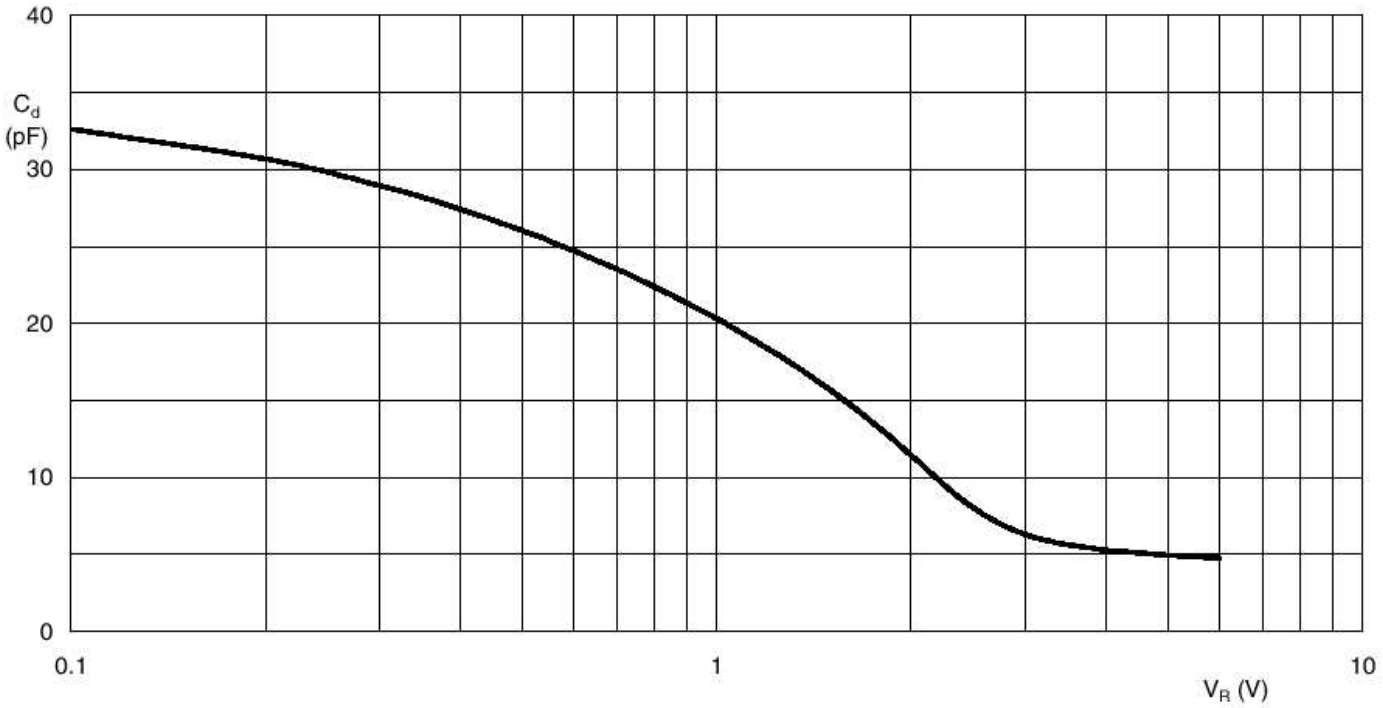
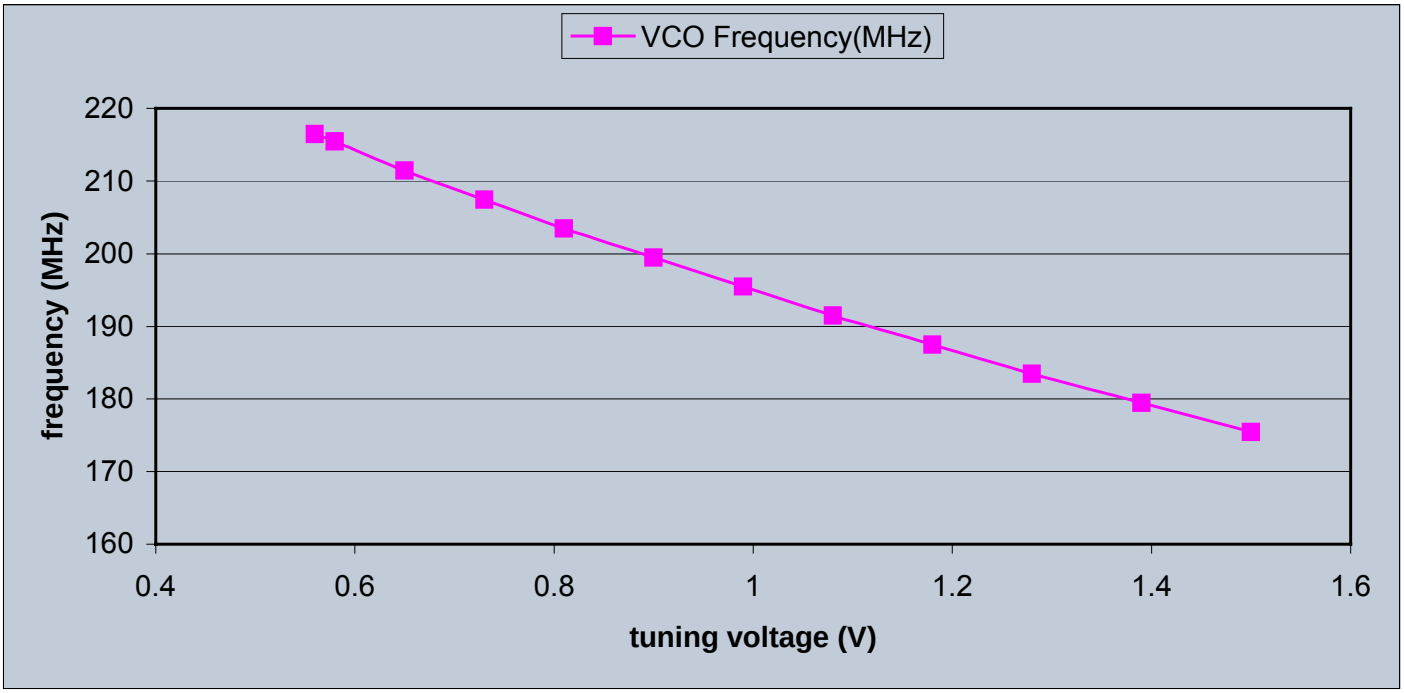


Figure 4 Diode Capacitance as Function of Reverse Voltage, Typical Values

Figure 5 Typical Oscillator Tuning Curve of Proposed FM Application



The inductance value of the oscillator coils L2 and L3 is about 33nH (Q=40 to 45). This inductance is very critical for the VCO frequency range and should have a low spread (2%). The quality factor Q of this coil is important for a large S/N ratio figure. The higher the quality factor the lower the noise floor VCO contribution at the output of the demodulator will be. With a quality factor between 40-45 a good compromise can be found between the size of the coil and the, by the oscillator determined, noise floor.

This is a shortened application note to emphasise the BB202 varicap as an important FM oscillator component next to the TEA5767/68 single chip stereo FM receiver (complete application note: AN10133).

Appendix C: Application note
RF switch for e.g. Bluetooth appl. (2.45 GHz T/R)

1 Introduction.

One of the most important building blocks for today's wireless communication equipment is a high performance RF switch. The switch main function is to switch an RF port (ANT) between the transmitter **(TX)** and the receiver **(RX)**. The most important design requirements are; low insertion loss **(IL)**, low inter-modulation distortion **(IMD)**, high isolation between TX and RX, fast switching and low current consumption – especially for portable communication equipment. This application note addresses a transmit and receive switch for 2.4 - 2.5 GHz, which is the unlicensed Industrial Scientific and Medical (ISM) band, in which the Bluetooth standard applies. The design demonstrates a high performance T-R switch utilizing low cost Philips BAP51-02 PIN Diodes as switching elements.

2 *p-i-n* Diode Switch Design.

There are a number of *p-i-n* diode based, single pole double throw (SPDT) topologies, which are shown in the Figures 1, 2 and 3. These topologies are widely used in RF and microwave design. They provide good performance, due to their symmetry and they show the same performance in both the RX and TX mode. The disadvantage of these topologies is the need for a pair of digital control signals and in both TX and RX mode a bias current is needed.

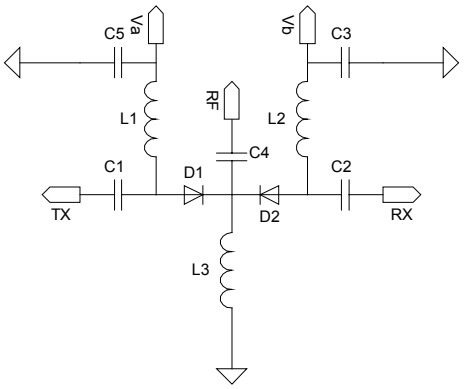


Figure 6. **SPDT switch with series diodes**

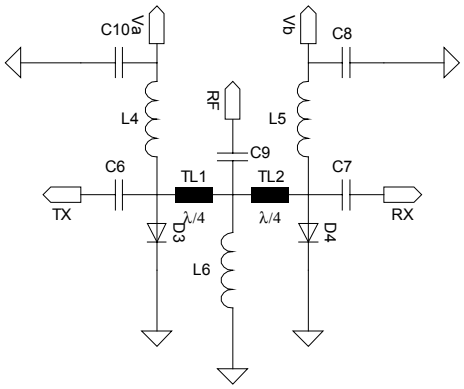


Figure 7. **SPDT switch with λ/4 sections to permit shunt diodes**

The topology we used for the design in this application note is shown in Figure 4. This is a combination of Figure 1 and 2. The design consists of a series-connected *p-i-n* diode, placed between the transmitter-amplifier and antenna, and a shunt-connected *p-i-n* diode at the receive port, which is a quarter-wavelength away from the antenna. In transmit mode both diodes are forward-biased with current. Both diodes are therefore in the low impedance state. Which means a low-loss TX-ANT path is combined with a RX port protected from the TX power.

The λ/4 transmission line transforms the low impedance at the RX port to a high impedance at the antenna. In the receive mode both diodes are ZERO biased (high impedance state), which results in a low loss path between antenna and receiver and high isolation ANT-TX path. One of the advantages of this approach is no current consumption is needed in the receive mode.

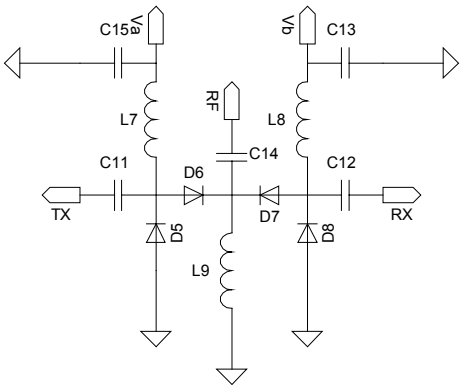


Figure 8. **SPDT switch with series shunt diodes which results in high isolation**

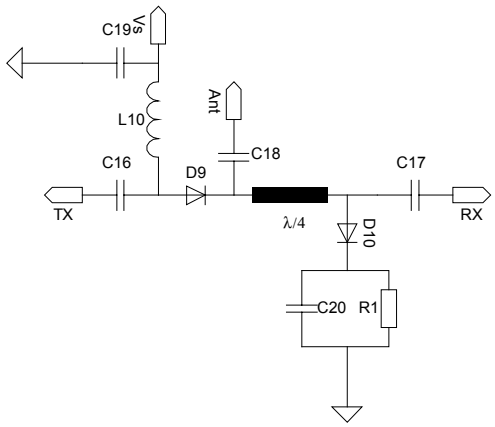


Figure 9. **SPDT switch with a combination of a series and a shunt connected PIN diode.**

The *p-i-n* diodes used in a switch like this should have low capacitance at ZERO bias ($V_R = 0V$) and low series resistance at low forward currents. The BAP51-02 typically shows 0.4 pF at 0V; measured at a frequency of 1 MHz and 2 Ω at 3 mA; measured at a frequency of 100MHz. For the shunt diode low series inductance is also required – 0.6 nH for the BAP51-02.

3 Circuit design.

Circuit and layout has been designed with the use of Agilent's Advanced Design System (ADS). The target performance of the switch is shown in Table 1.

Mode	RX (0V)	TX(3mA)
Insertion Loss	< 0.65 dB	< 0.8 dB
Isolation TX/RX	>18 dB	>14.5 dB
Isolation RX/Ant	>16.5	-
Isolation TX/Ant	-	>14.5dB
VSWR RX	<1.2	-
VSWR TX		<1.3
VSWR Ant	<1.2	<1.3
Power handling	+20dBm	+20dBm
Current consumption		3mA @ 3.7V

Table 1

The ADS circuit of the switch is shown in Figure 5. Note that D1 is series connected with the *p-i-n* diode in the receive path and D2 is connected in shunt in the receive RF path. DC bias current is provided through inductance L1, and limited to about 3mA by resistor R1 = 680 Ω. Notice also that the λ/4 microstripline (width 1.136mm, length =16.57mm) is divided into several sections in order to save some board space. All the footprints for the SMD components have been modeled as a gap and a piece of stripline in order to approach the actual practice of the design on PCB.

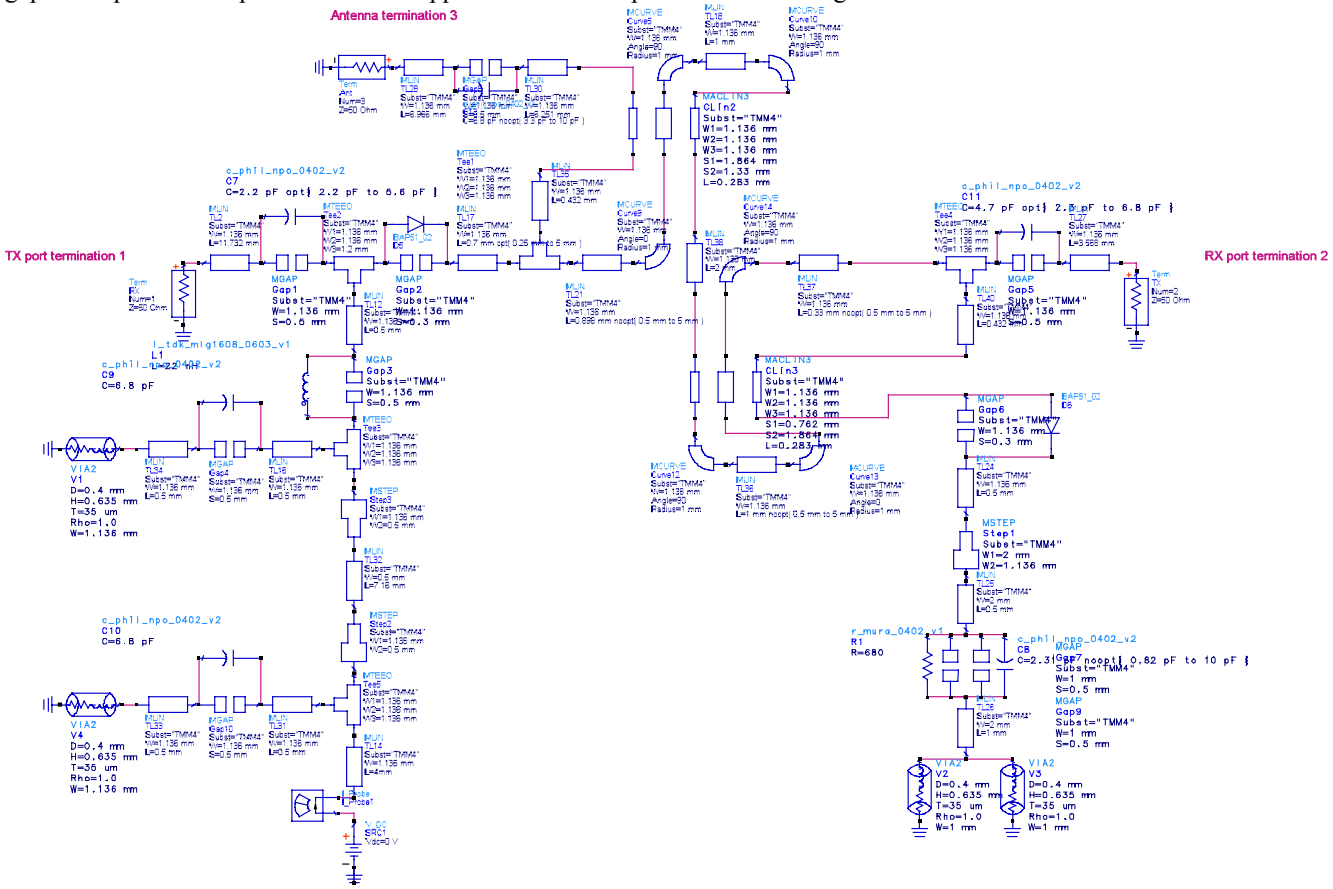


Figure 10 ADS circuit file

The discontinuity effects of the microstrip to coaxial interface have not been taken into account.

4 BAP51-02 Model.

The Silicon *p-i-n* diode of the Philips Semiconductor BAP51-02 is designed to operate as a low-loss, high-isolation switching element and is capable of operating with low intermodulation distortion.
The model for the BAP51-02 PIN diode for an ADS environment is shown in Figure 6. The model consists of two diodes, in order to achieve a fit on both DC and RF behavior. Diode D1 is used to model the DC voltage-current characteristics, Diode D2 is the *p-i-n* diode built-in model of ADS and is used to model the RF resistance versus DC current behavior of the *p-i-n* diode-model. Both diodes are connected in series to ensure the same current flow. For RF the *p-n* junction Diode D1 is shorted by an ideal capacitor (DC block), while the portion of the RF resistance, which reflects the residual amount of series resistance is modeled with R1 = 1.128 Ω. To avoid affecting the DC performance this resistor is shunted with the ideal Inductor (DC feed).

Capacitance C2 and inductors L2 and L3 reflect package parasitics. The described model is a linear model that emulates the DC and RF properties of the *p-i-n* diode from 6 MHz up to 6 GHz.

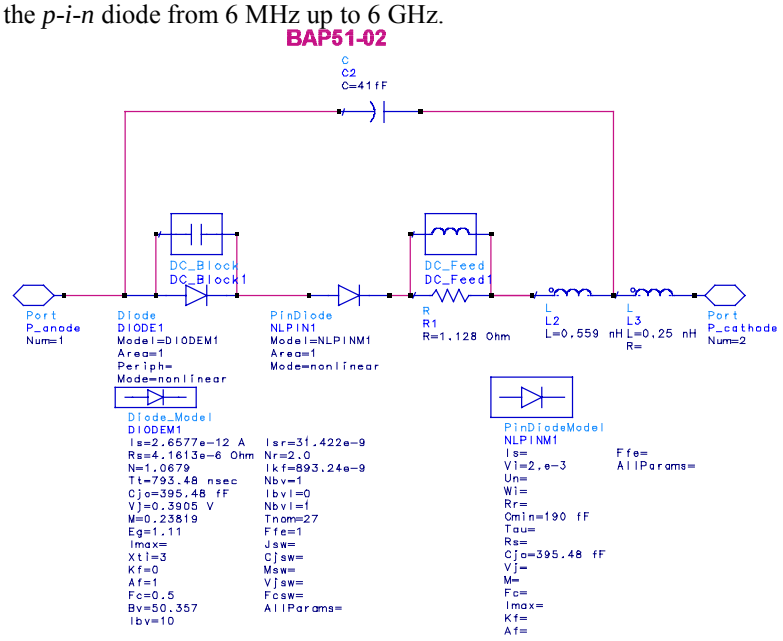


Figure 11; BAP51-02 Small Signal Model for an ADS environment

5 Circuit and Layout Description

The circuit diagram for the switch is shown in figure 7 and the PC board layout is shown in Figure 8. The bill of materials for the switch is given in Table2. The PC board used was 0.635mm thick using FR4 material ($\varepsilon_r = 4.6$). Copper plane on both sides was 35 µm thick copper and overlaid with 3 µm gold plating. On the test board SMA connectors were used to feed the RF signals into the board.

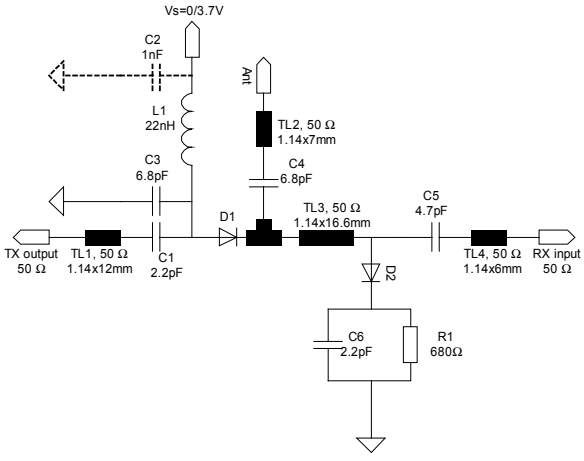


Figure 12; circuit diagram

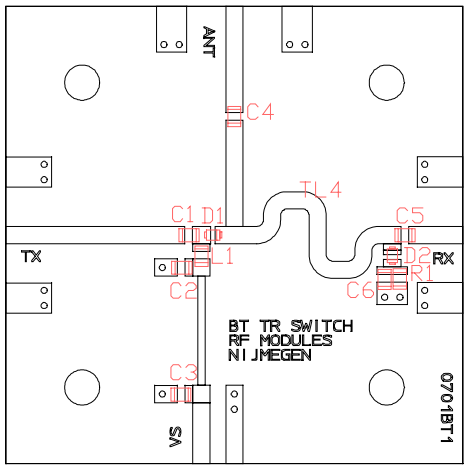


Figure 13; PC board Layout.

Component	Value	Footprint	Manufacturer
C1	2.2 pF	0402	Philips
C2*	1 nF	0402	Philips
C3	6.8 pF	0402	Philips
C4	6.8 pF	0402	Philips
C5	4.7 pF	0402	Philips
C6	2.2 pF	0402	Philips
R1	680 Ω	0402	Philips
D1	BAP51-02	SC79	Philips
D2	BAP51-02	SC79	Philips
L1	22 nH	1005	Taiyo yuden
TL1	λ/4;50 Ω		on the PCB

Table 2 Bill of materials *C2 is optional.

6 Measurement results.

In Table 3 the measured performance of the switch is summarized. In Figure 9 both the simulation and measurement results in TX mode (3.7V/3mA) are shown. The RX mode measurement results can be seen in Figure 10.

	Mode	
Parameter	RX (0V)	TX(3mA)
Insertion Loss @ 2.45GHz	< 0.57 dB	< 1.0 dB
Isolation TX/RX @ 2.45GHz	>20.4 dB	>23.6 dB
Isolation Ant/RX @ 2.45 GHz	-	>23.5 dB
Isolation TX/Ant @2.45 GHz	>19.76 dB	-
VSWR RX @2.45 GHz	1.24	-
VSWR TX @2.45 GHz	-	1.35
VSWR Ant @2.45 GHz	1.19	1.29
IM3 p-i-n 0 dBm f1=2.449 GHz f2=2.451 GHz	+39 dBm	+40 dBm
IP3 p-i-n 0 dBm f1=2.449 GHz f2=2.451 GHz	+43.8 dBm	+44.8 dBm
IM3 p-i-n +20 dBm f1=2.449 GHz f2=2.451 GHz	+38.5 dBm	+39.5 dBm
IP3 p-i-n +20 dBm f1=2.449 GHz f2=2.451 GHz	+43.3 dBm	+44.3 dBm
Power handling	+20 dBm	+20 dBm
Current consumption		3mA @ 3.7V

Table 3 measured switch performance.

Intermodulation distortion measurements were performed as follows. In both RX and TX state the measurements were first done with two input-signals, each at 0 dBm and second set of signals at +20 dBm. In transmit state these signals were applied to the TX port, distortion was measured at the antenna port, while the RX port was terminated with 50Ω. In receive state the two signals were applied to the ANT port, distortion was measured at the RX port, with the TX port terminated.

According to reference 2, the third order harmonic distortion product is 9.54 dB less than the third order intermodulation product. The third order harmonic intercept point IP3 is 9.54/2 higher than the third order intermodulation intercept point IM3.

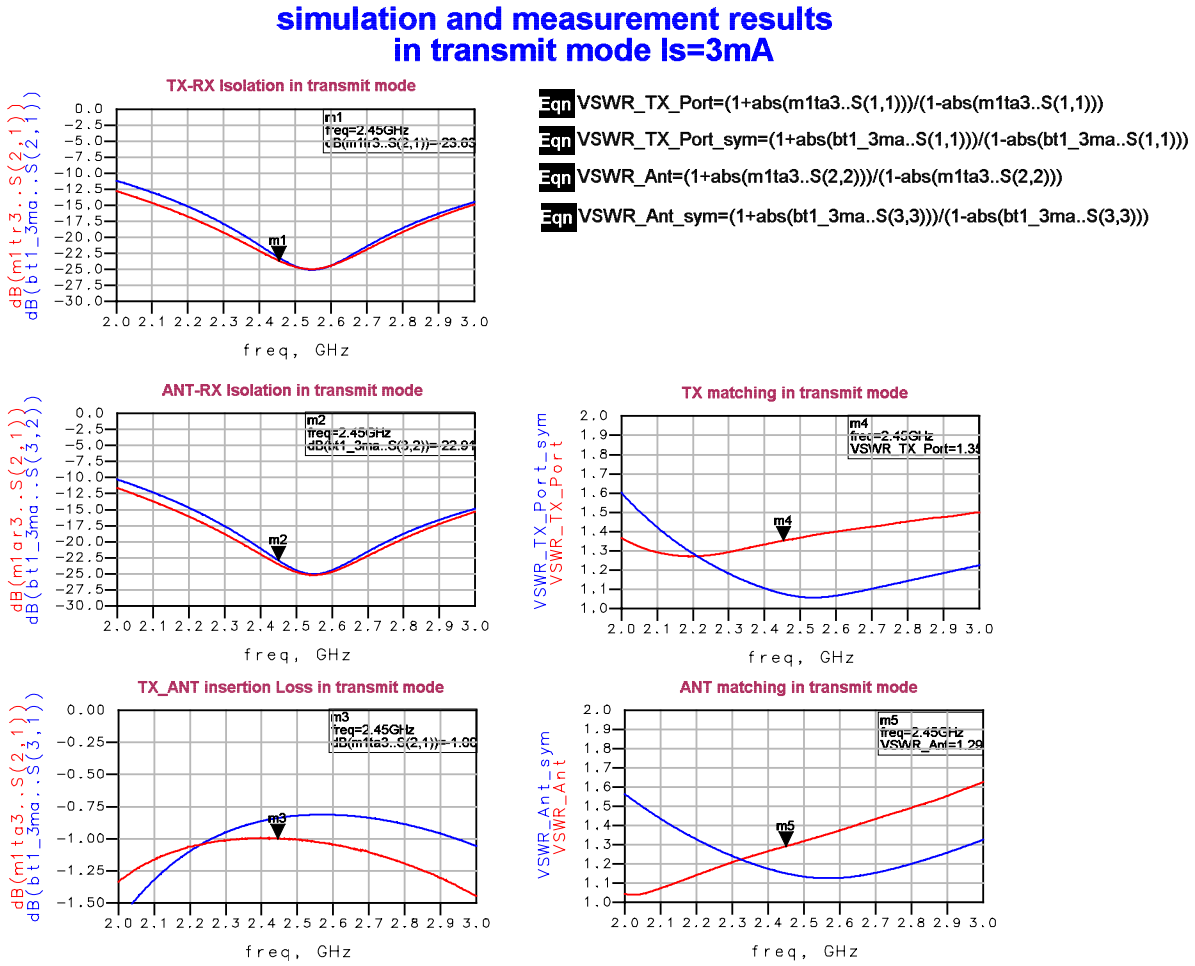


Figure 14; Results in TX mode; red curves are measurements, blue curves are the simulated ones.

Remark: *Loss and isolation results are all including approximately 0.2 dB loss of the SMA connectors which were used to fed the RF signals through the design. This has a great impact on the insertion loss results.*

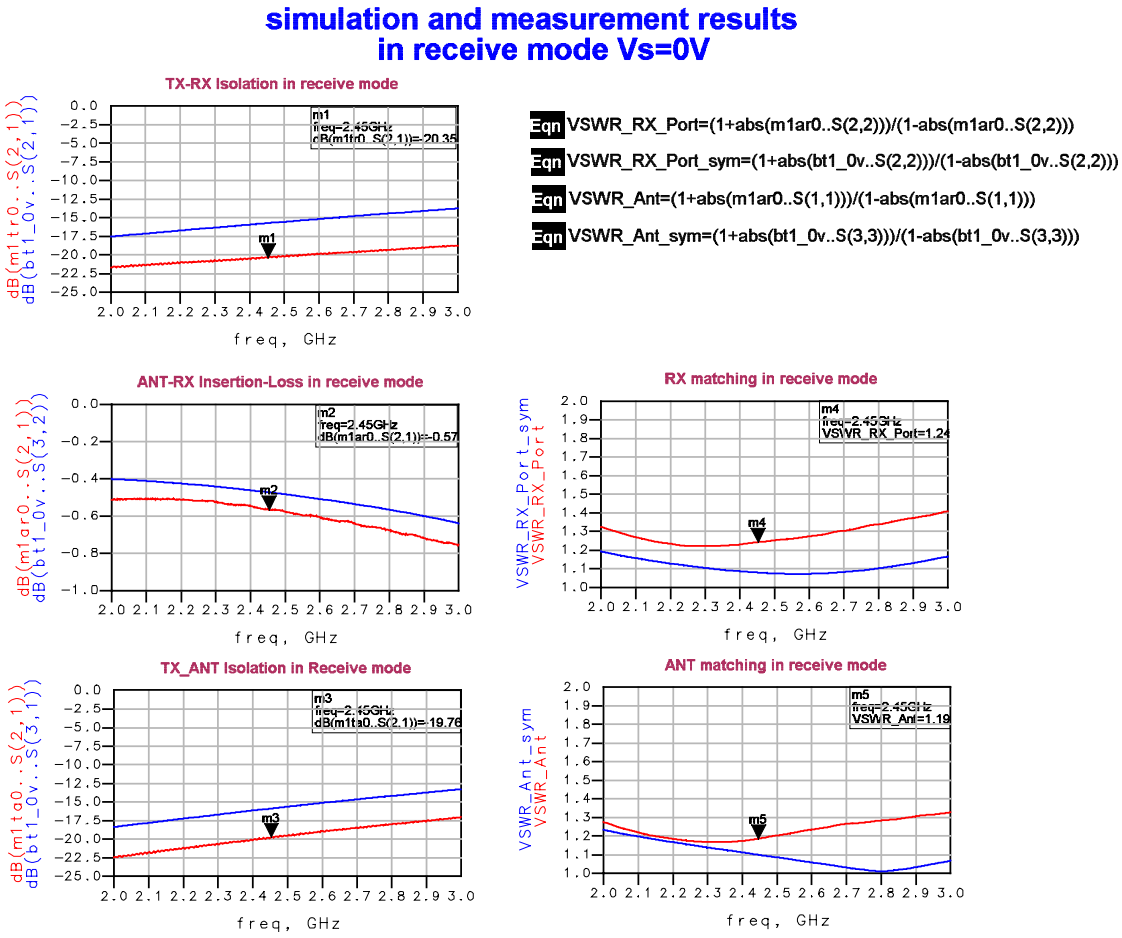


Figure 15; Results in RX mode; red curves are measurements, blue curves are the simulated ones

Remark: *Loss and isolation results are all including approximately 0.2 dB loss of the SMA connectors which were used to fed the RF signals through the design. This has a great impact on the insertion loss results.*

Recommendations.

1 In this design the BAP51-02 was used because it's designed for switching applications related to insertion loss and isolation. When a better IM distortion is required it is better to use the BAP64-02 from Philips Semiconductors.

2 As can be seen the λ/4 section requires a lot of boards space. This section could be replaced by a lumped element configuration, which results offers board real estate savings.

References:

1; Gerald Hiller, "Design with PIN diodes," App note APN1002 Alpha industries inc.

2; Gerald Hiller, "Predict intercept points in PIN diode switches," Microwaves & RF, Dec. 1985.

3; Robert Caverly and Gerald Hiller, "Distortion in PIN diode control circuits," IEEE Trans on Microwave

Appendix D: Application of the RF Switch BF1107/8 Mosfets

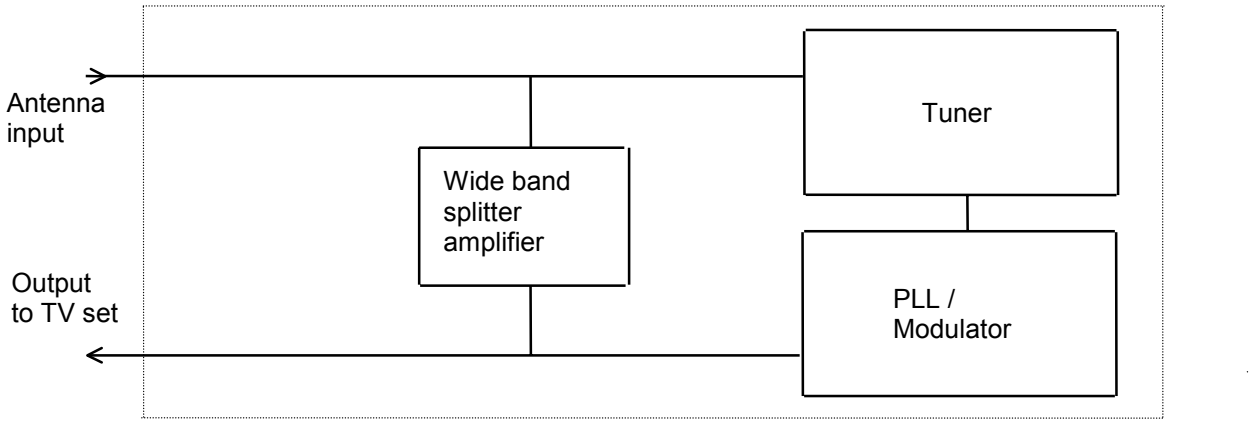
APPLICATION OF THE RF SWITCH BF1107

INTRODUCTION

If a (Mos)fet is used in its linear region, it can be used as a variable resistor. The resistance depends on the bias voltage between Gate and Source and the pinch - off voltage of the Mosfet.
If the bias voltage is lower than the pinch - off voltage the resistance of the Mosfet is infinite. If the bias voltage is much higher than the pinch - off voltage the resistance of the Mosfet is low.
Due to this a Mosfet can be used as a switch.
At low Gate - Source voltages the Mosfet is switched off and at high Gate - Source voltages the Mosfet is switched on.
If a Mosfet is used with relatively low capacitances the Mosfet can be used as an RF switch. With this Rf switch, RF signals can be switched off and on.
The BF1107 is a triode Mosfet intended for switching RF signals.
If the Drain - Source voltage is set to 0V, this Mosfet is biased in its linear region.
This Mosfet has a pinch - off voltage of approx. 3V.
Therefore this Mosfet is switched on if the Gate - Source voltage is 0V. Together with a Drain - Source voltage of 0V this means that the Mosfet is switched on if all bias voltages are 0V.
If the Gate - Source voltage is set to a value lower than 3V this Mosfet is switched off.

APPLICATION IN A VIDEO RECORDER

A block diagram of the principle circuit of the RF front end of a VCR is given in Fig.1 below.



If the VCR is not used (“stand-by”) at least the wide band splitter amplifier must always be switched on to ensure reception of TV signals in the TV set. Power consumption in stand-by can be reduced if the supply voltage of the VCR can be switched off, but special measures must be taken to ensure the reception of TV signals.
This can be done by connecting a switch between the input and output. (See Fig. 2 below). This is a so called “Passive Loop Through”.

To reduce power consumption the switch must be:

- on if the VCR is switched off and
- off of the VCR is switched on.

This switching can be done with a Mosfet. (See Fig. 3 below).

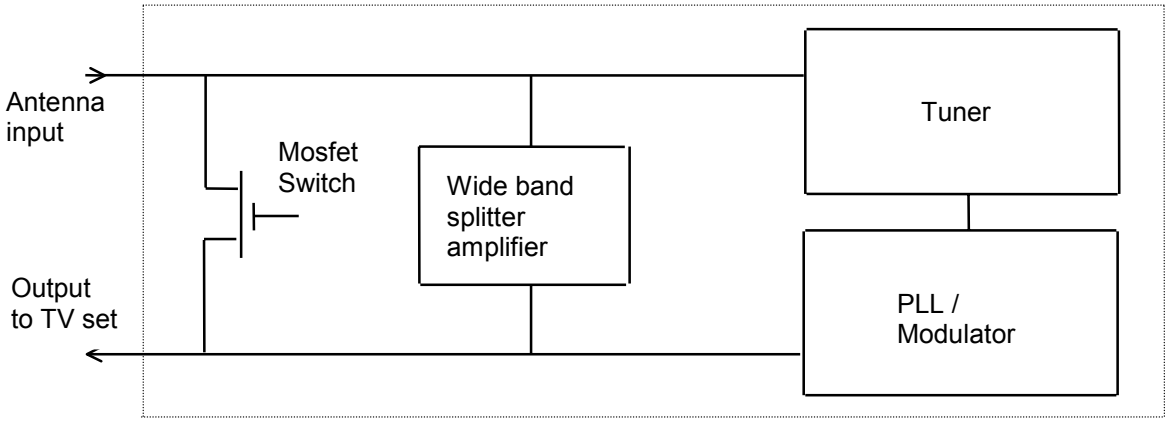


Fig. 3

If for the switch a depletion type Mosfet is chosen then this Mosfet is switched on if all the supply voltages at the Mosfet are 0.
The Mosfet is switched off if the Gate - Source voltage has a negative value more negative than the pinch-off voltage of the Mosfet.

If the supply voltage of the VCR is switched on the Mosfet switch must be switched off. This can be done by connecting the Drain and the Source of the Mosfet to the supply voltage and connecting the Gate to ground.
The principle of this is given in Fig. 4 (next page).
If the supply voltage = 0, than the Drain-, Source- and Gate voltages of the Mosfet switch are 0. Than the antenna signal flows through the Mosfet switch to the TV set. If the supply voltage = 5V, then the Drain and Source voltages of the Mosfet switch are 5V. The capacitor C ensures that the Drain and the Source voltages are equal. The Gate voltage is 0 (Gate is grounded).

Then the antenna signal flows through the VCR as usual.

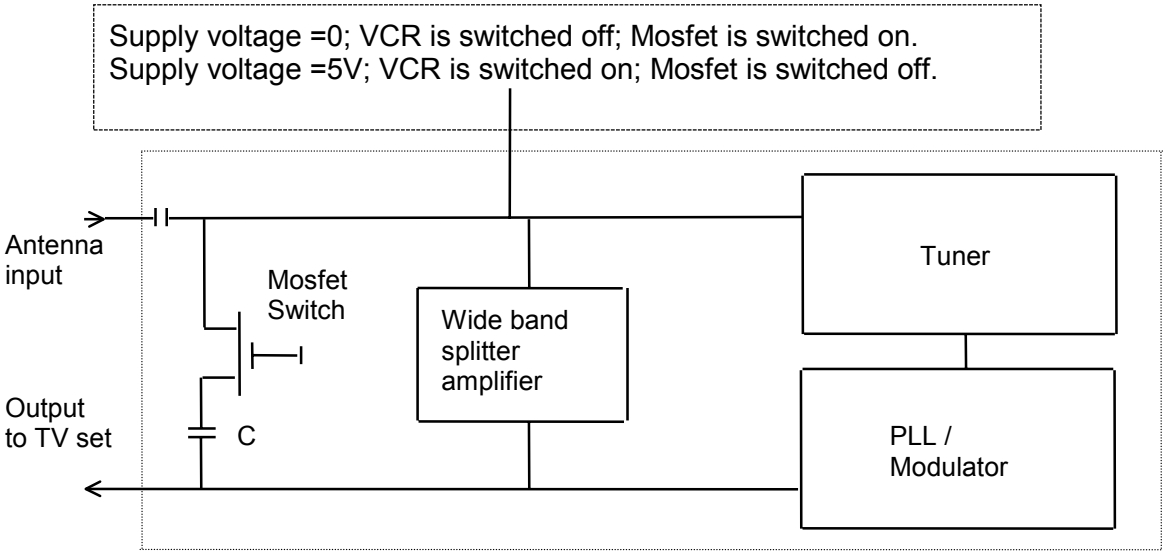
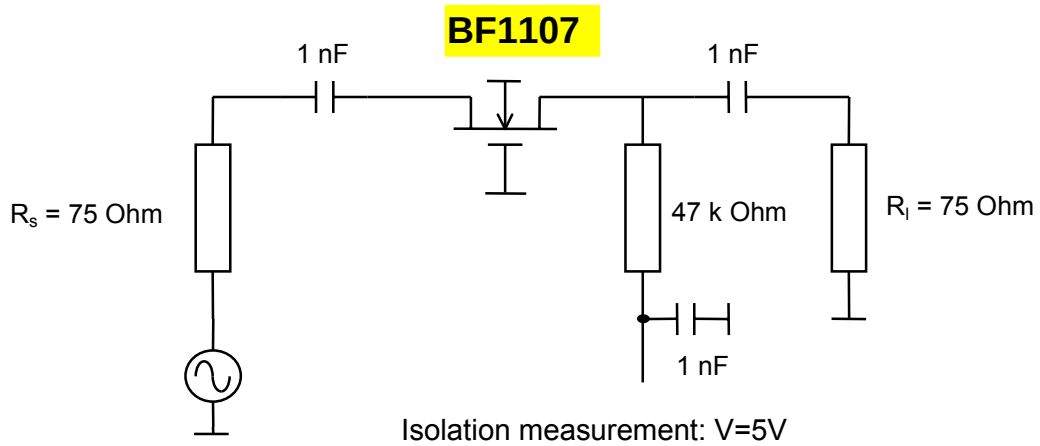


Fig. 4

For the Mosfet switch in this circuit a BF1107 can be applied. In the on state of the switch the losses must be low, because losses determine, for a large amount, the increase of the noise figure of the TV set. In the off state the isolation must be high because the oscillator signal from the modulator must be kept very small at the antenna input.
The main advantage of applying the BF1107 as a switch for the passive loop through is that this Mosfet uses no current. Not in the on state, nor in the off state. Switching is done only with voltages.

PERFORMANCE OF THE BF1107

The performance of the RF switch was measured in a circuit as given in Fig. 5.



Isolation measurement: V=5V
Losses measurement: V=0V

In this circuit we measured isolation and losses as a function of frequency.
The results of these measurements are given in Fig. 6.

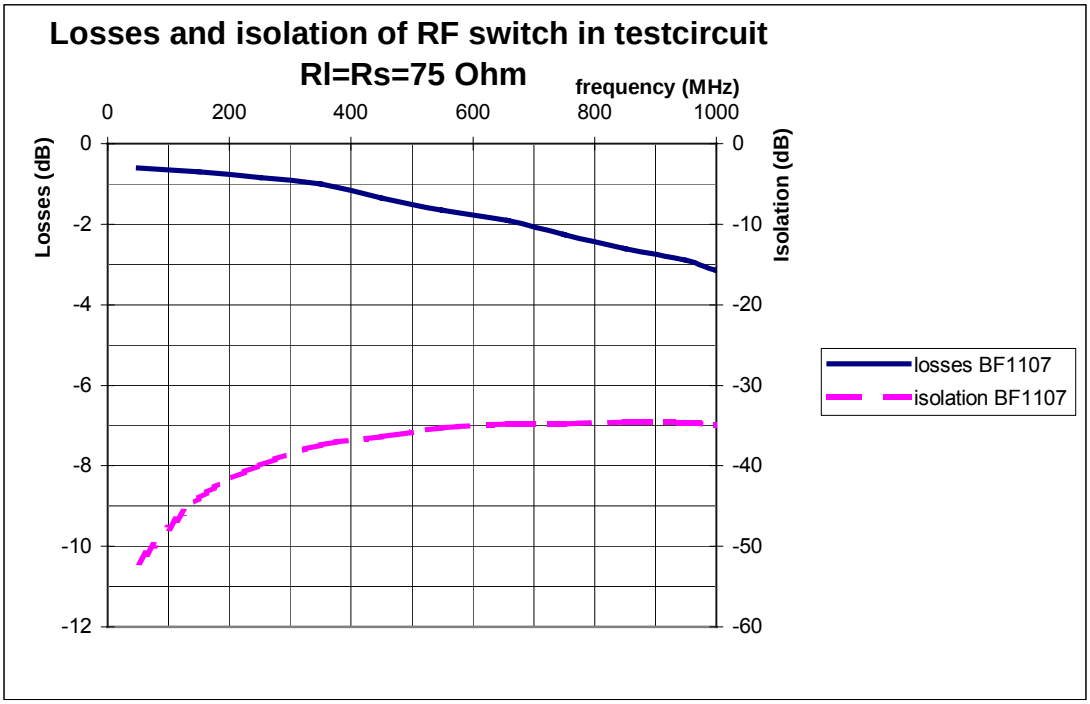


Fig. 6

The isolation (Mosfet is switched off) in the testcircuit is mainly determined by the feedback of the Mosfet in common Gate plus the parasitic capacitance of the testcircuit between Drain and Source. This parasitic capacitance must be very small.
The losses (Mosfet is switched on) in the testcircuit are at low frequencies determined by the $R_{DS\ on}$ of the Mosfet and at high frequencies by the $R_{DS\ on}$ and the Drain - Gate and Source - Gate capacitances of the Mosfet.
The parasitic capacitances of the circuit must be kept much lower than the capacitances of the Mosfet.

SPECIAL MEASURES TO BE TAKEN

In Fig. 4 only the principle of the application circuit of the switch in the VCR is given.
In the practical application circuit of a VCR the input and output of the wide band splitter amplifier are connected to the input and output of the switch.
As stated in chapter 3 the losses in the on situation of the switch are also determined by the capacitances at the input and the output of the switch.
If in the principle circuit of Fig.4 the Mosfet is switched on, then the wide band

splitter amplifier is still connected to the RF switch. This results into higher losses. Therefore special measures are needed to reduce the influence of the presence of the amplifier on the losses.
Theoretically this can be done by disconnecting the input as well as the output of the amplifier from the switch.
In practice this disconnecting can be done with a switch.
The principle of the circuit is then as given in Fig. 7.

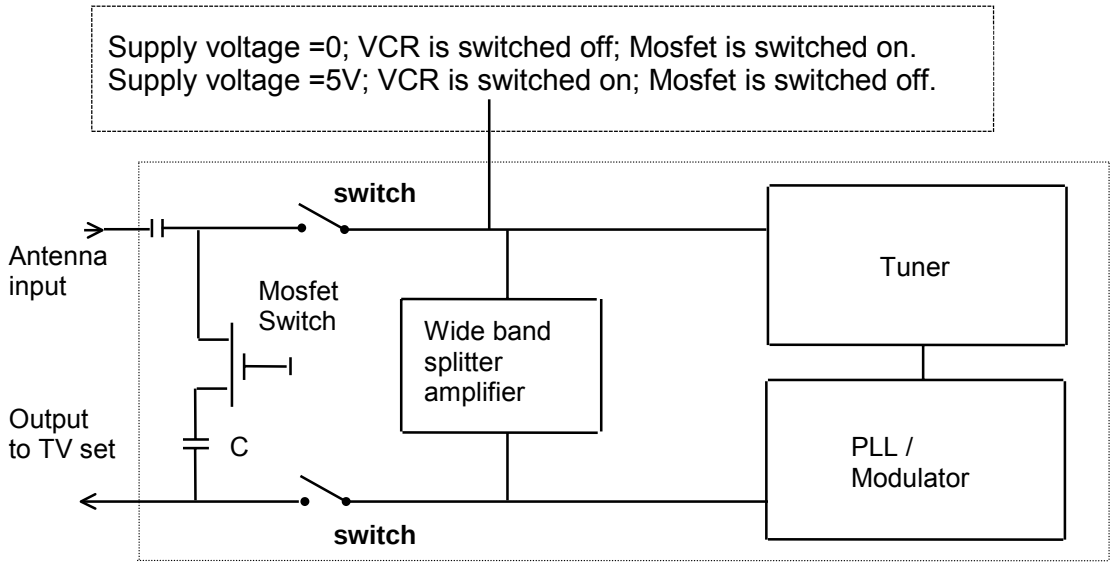


Fig. 7

The losses of the two switches in Fig. 7 must have low resistance if this switch is on and low capacitance if this switch is off. Such switches can be made with diodes. With the right choice of the diodes the resistance is low if the diode is forward biased and the capacitance is low if the bias voltage of the diode is 0V. Diodes that can be applied are bandswitching diodes (e.g. BA792 or BA277).
If the two stages of the wide band splitter amplifier are biased via the diode switches then the amplifier is “disconnected” from the switch if the supply voltage is 0V and “connected” if the supply voltage is 5V.
The main part of the circuit is then as given in Fig. 8 next page.

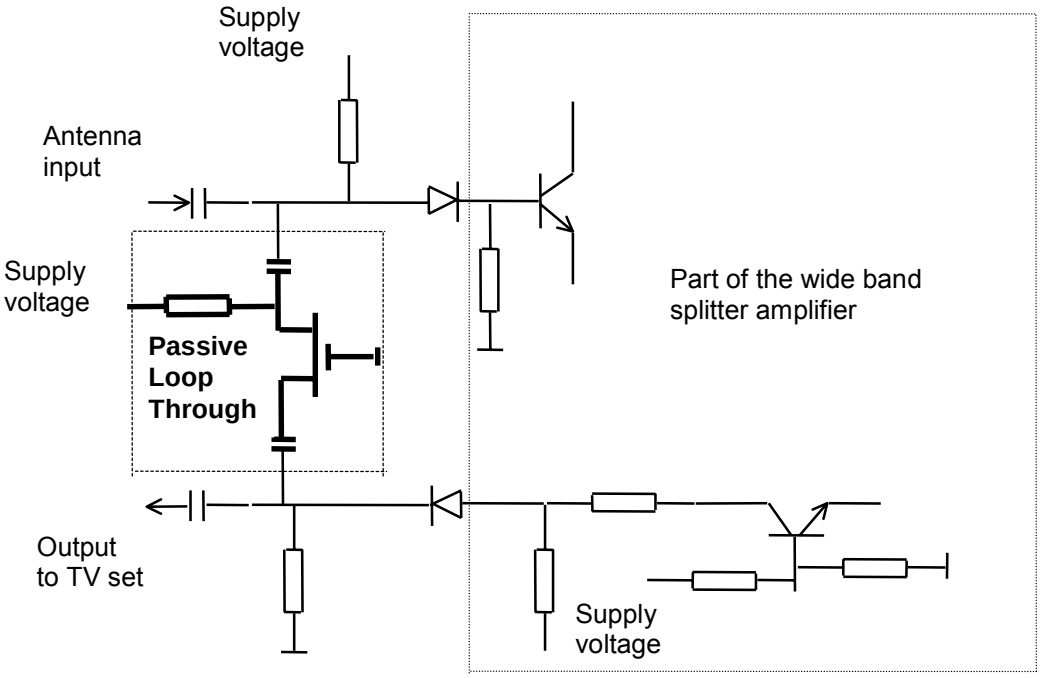


Fig. 8

CONCLUSIONS

The BF1107 is a specially developed triode Mosfet for the application of RF switch. In the on condition of the switch as well as in the off condition no D.C current flows through the Mosfet.
One of the application areas is the “Passive Loop Through” in a VCR.
The requirements for this application are:

Losses:	typ 2dB	max. 4dB.
Isolation:	> 30dB.	

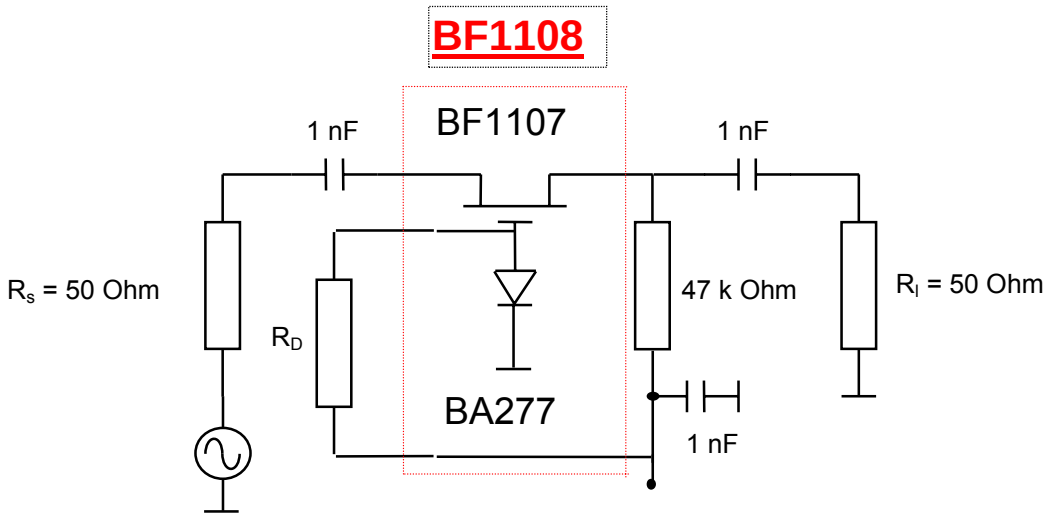
This can be achieved with a BF1107 in the circuit of Fig. 8.
If this switch is applied the supply voltage of the VCR can be switched off in the “stand - by” condition of the VCR.
The R.F signal path to the T.V. set is then via the switch and not via a (power consuming) wide band splitter amplifier.

APPLICATION OF THE RF SWITCH BF1108

(BF1107 + BA277 in a SOT143 package)

INTRODUCTION

The BF1108 is a small signal RF switching Mosfet that can be used for switching RF signals up to 1GHz with good performance and switching RF signals up to 2GHz with reasonable performance. (See Fig. 1 for the circuit diagram).



Isolation measurement: V_{supply}=5V
Losses measurement: V_{supply}=0V

Fig. 1

The BF1108 consists of the RF switch BF1107 with a diode BA277 connected in series with the Gate. Drain and Source are interchangeable.
Both, the BF1107 and BA277 were mounted in one SOT143 package.

RF SWITCH BF1108 IN ITS APPLICATION

The losses of the RF switch are determined by the on resistance of the BF1107 and the capacitances at the input and the output to ground.
If no supply voltage is present at the RF switch (switch is on) than the gate of the BF1107 is connected to ground via the small capacitance of the diode BA277.
This will result in improved losses, especially at high frequencies. This is because input and output capacitance of the switch are lowered.

The isolation of the RF switch is determined by its' off resistance in parallel with the feedback capacitance and the impedance between gate and ground.
If there is a 5V supply voltage present at the switch (switch is off) than the gate of the BF1107 is connected to ground via the small seriesresistance of the BA277.
The impedance between gate and ground is mainly determined by the inductance from gate to ground, especially at high frequencies. Therefore the small extra series resistance of the BA277 will have marginal influence on the isolation of the switch. However, the extra series inductance has influence on the isolation, especially at high frequencies.
For the BF1107 no current is needed as well in the on state as in the off state.
For the BF1108 also no current is needed for the on state. In the off state a small current through the BA277 is needed to ensure relatively low series resistance.

MEASUREMENTS ON THE BF1108

On the BF1108 we have measured the losses in the on state (V_{supply} = 0V) and the isolation in the off state (V_{supply} = 5V) in a 50Ω test circuit (see Fig. 1).
For comparison we have also measured the losses and the isolation of a BF1107.
The results of the measurements on a BF1107 are given in Graph. 1.
The results of the measurements on a BF1108 are given in the Graphs. 2 and 3.
In Graph 2 the results are given with a bias resistor (to the BA277) of 4.7kΩ.
This is a d.c. forward current through the diode of appr. 1mA.
Graph 3 shows the results with a d.c. current through the diode of appr. 2mA.
(Bias resistor to the diode 2.2kΩ).
In the specification the losses and the isolation are specified up to 860MHz.
However, it is possible to use the BF1108 also at higher frequencies with somewhat less performance. For information we have also measured the BF1108 and BF1107 at frequencies up to 2.05GHz.
The results of these measurements are given in Graph 4.

INFLUENCE OF PARASITIC CAPACITANCES

It is obvious that parasitic capacitances will influence the performance of the RF switch, also, additional feedback as well as additional parallel capacitances in parallel with the BF1108.
Measurements are done with additional parallel capacitances between Drain and Ground and between Source and Ground (see Fig. 2, next page).
We have also added some additional feedback between Drain and Source.
The results of these measurements are given in Graph 5.

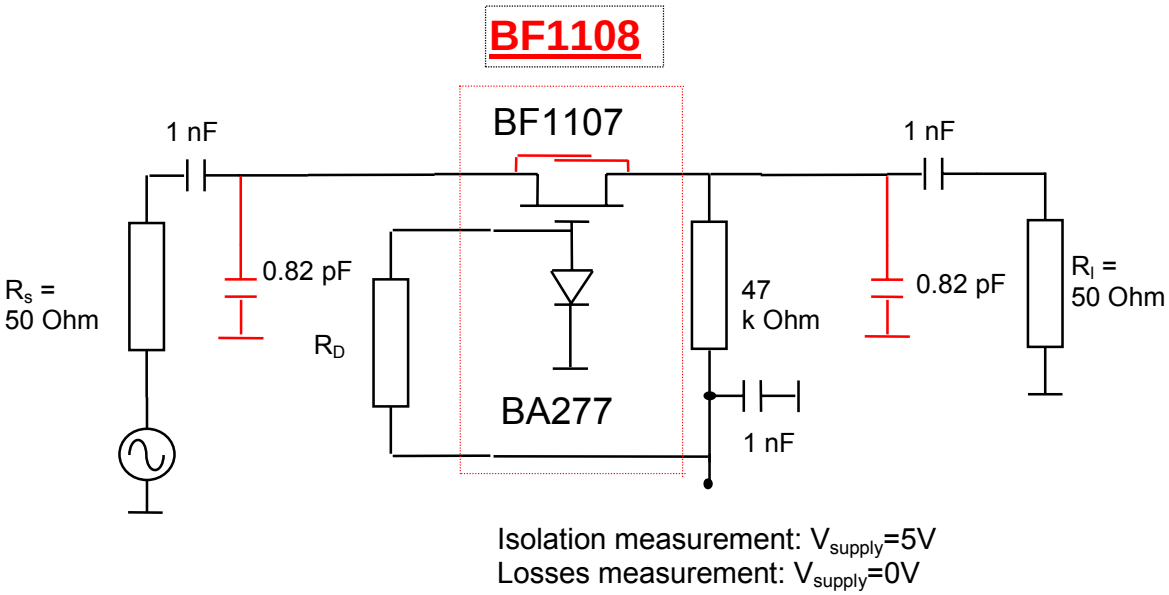
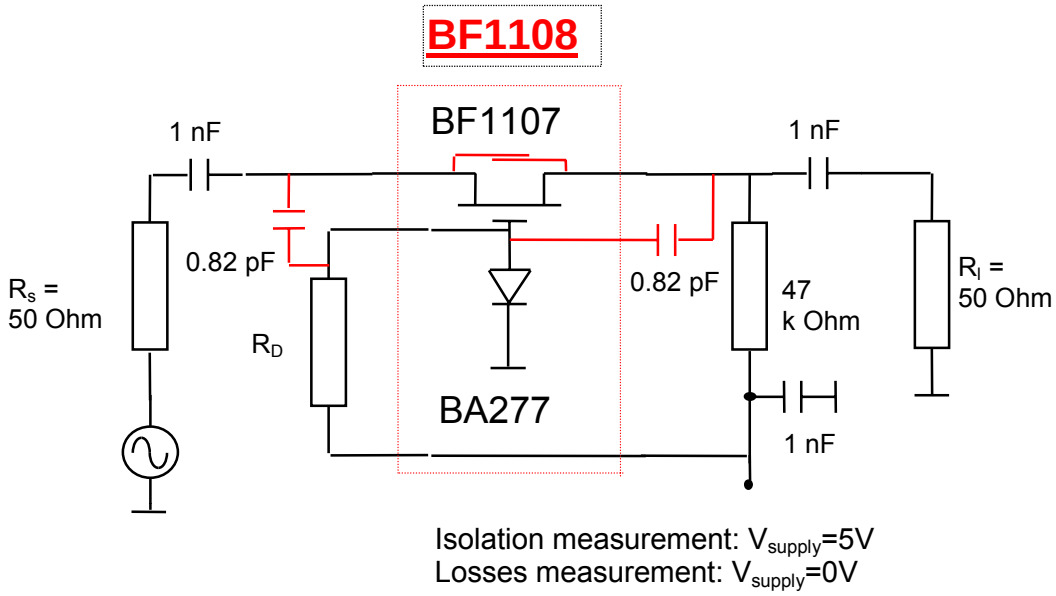


Fig. 2

The additional feedback was made by a short wire connected to the Drain, bending it towards the Source.

We have also done measurements with additional capacitances between Drain and Gate and between Source and Gate. Also with additional feedback between Drain and Source. Than the circuit diagram is as given in Fig. 3.



DISCUSSION ABOUT THE MEASURED RESULTS

Comparison of graphs 1, 2 and 3 show that at 1GHz the losses have been improved by appr. 0.5dB if a BF1108 is used i.s.o. a BF1107. Graph 4 shows that the BF1108 can also be used at frequencies higher than 1GHz with relatively reasonable performance. The losses at 2GHz are appr. 2.4dB for a BF1108 and > 5dB for a BF1107. At frequencies > 1GHz the isolation of a BF1108 is worse compared to that of the BF1107. This is caused by the seriesinductance of the BA277 (with bonding wires) to ground. If additional parallel capacitance is present at the input and the output of the BF1108 (Graph 5) the losses increase. We have done measurements with 0.82pF added. This increases the losses at 1GHz to appr. the same value as with the BF1107. This is because the advantage of the BF1108 with respect to the BF1107 is a reduction of the capacitance to ground if the switch is on and for these measurements we have increased this capacitance. The additional feedback capacitance results as can be expected in worse isolation and has almost no influence on the losses.
An explanation for this behaviour can be given with the help of the Figs. 4 and 5 which are simplified circuit diagrams of the BF1108 in the on state and off state respectively.

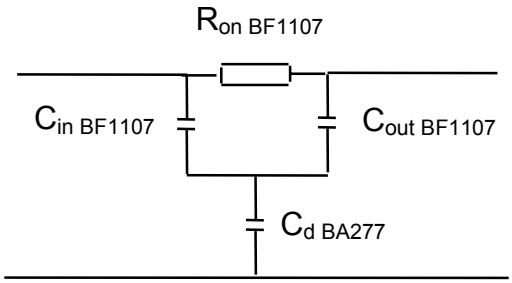


Fig. 4: Simplified circuit diagram of the BF1108 in the on state.
The losses in this circuit are mainly determined by the R_{on} of the BF1107, especially if the capacitance of the BA277 is small. If parallel capacitances at the input and output are present this will result in additional signal loss, especially at high frequencies. A small additional feedback capacitance in parallel with the relatively low ohmic R_{on} will have no influence on the losses.

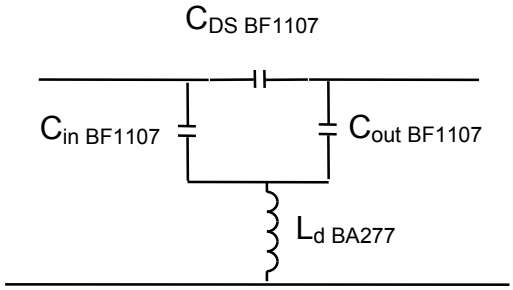


Fig. 5: Simplified circuit diagram of the BF1108 in the off state.
The isolation in this circuit is not only determined by the signal transfer via the feedback capacitance C_{DS} but also by the signal transfer via C_{in}, L_d and C_{out}. These two kinds of signal transfer have (roughly) opposite phases.

If the signal transfer is only determined by the feedback capacitance one would expect a decrease in the isolation with 6dB / octave (if $1/\omega C_{DS} << (R_s + R_l)$. However, due to the opposite phases of the two signal transfers there will be a dip in the graph for the isolation as a function of frequency. In the Graphs 2, 3, 4 and 5 this dip is present at about 950MHz if no additional feedback is present. If additional feedback is present the dip shifts to a higher frequency. More series inductance in the Gate shifts the dip to a lower frequency. This can be seen from Graph 4 where the BF1107 and BF1108 are compared. For the BF1107 the dip is present at appr. 1850 MHz. The BF1108 shows a dip at appr. 950MHz. Due to this the isolation of the BF1108, compared to that of the BF1107, is worse at frequencies > 1GHz..

If additional capacitance (0.82pF) is present between Drain and Gate and Source and Gate, then the losses increase by appr. 0.25dB at 1GHz. This can also be explained from the fact that the capacitive signal path to ground is lower ohmic than without this additional capacitance. The influence of additional capacitances is much lower than connecting them directly to ground. This is because of the presence of the small diode capacitance. The isolation as a function of frequency is very dependent on the presence of the additional capacitances. (Compare Graph 3 and 6). We see that the dip in the curve is shifted to appr. 650MHz. And now the isolation at 1GHz is worse than 30dB. As stated before the dip can be shifted to a higher frequency if additional feedback is present. Than the dip can again be set to appr. 950MHz. The isolation at lower frequencies is than worsened, but now at 1GHz an isolation of > 30dB can be achieved (see Graph 6). Additional feedback does not influence the losses.

CONCLUSIONS

The BF1108 is an RF switch which has low losses at frequencies up to 2GHz. In the on state the losses are 1.15dB typical at 50MHz slowly increasing to 1.4dB typical at 1GHz and 2.4dB typical at 2GHz. The losses are strongly dependent on additional parallel capacitances present at the input and the output of the switch and almost not dependent on additional feedback between Drain and Source. The isolation of the BF1108 is > 50dB at 50MHz decreasing to appr. 35dB typical at 1GHz and appr. 15dB typical at 2GHz. The Graphs for the isolation as a function of frequency show a dip at a certain frequency. This dip is caused by a compensation effect of a signal transfer via the Drain - Source feedback capacitance and a signal transfer via the input- and output capacitances and the series inductance in the Gate. These two signal transfers have opposite phase which causes the dip in the curve. From this we can also conclude that the losses are strongly dependent on the feedback capacitance, the Drain - Gate and the Source - Gate capacitances and the series inductance in the Gate. Additional feedback capacitance shifts the dip in the curve isolation as a function of frequency to a higher frequency. The isolation at low frequencies is than worsened. Additional capacitances between Drain and Gate and Source and Gate and more series inductance in the Gate shifts the dip to lower frequencies.

Appendix E: Application Note MOSFET

1. **INTRODUCTION**

At Philips we have different types of Dual Gate MOSFETs.
Our preferred types for use in television tuners are:

the 12V types	in SOT143:	BF998, BF908,BF1100
	in SOT143R:	BF998R, BF908R,BF1100R
	in SOT343R:	BF998WR, BF908WR,BF1100WR
the 9V types	in SOT143:	BF1100, BF1109
	in SOT143R:	BF1100R, BF1109R
	in SOT343R:	BF1100WR, BF1109WR
and also for 9V the	BF998, BF998R, BF998WR,	BF908, BF908R and BF908WR

with somewhat worse performance compared to the 12V application.

and the 5V types	in SOT143:	BF904, BF904A, BF909, BF909A, BF1101, BF1105, BF1201, BF1202
	in SOT143R:	BF904R, BF904AR, BF909R, BF909AR, BF1101R, BF1105R, BF1201R, BF1202R
	in SOT343R	BF904WR, BF904AWR, BF909WR, BF909AWR BF1101WR, BF1105WR, BF1201WR, BF1202WR and
the 2 in 1 MOSFETs	in SOT363:	BF1102, BF1102R, BF1203, BF1204

The types BF998((W)R) and BF908((W)R) have no integrated bias.
The types BF904((W)R), BF909((W)R), BF1100((W)R), BF1101((W)R), BF1201((W)R), BF1202((W)R), BF1102(R), BF1203 and BF1204 have partly integrated bias.
The types BF1105((W)R), and BF1109((W)R), have fully integrated bias.
As a consequence the external bias circuits of the different MOSFETs are different.
The BF998((W)R) and the BF904((W)R) are MOSFETs with relatively low transconductance ($Y_{fs\ typ}$ ~ 24 - 25 mS) and capacitances ($C_{is\ typ}$: 2.1 - 2.2 pF). The BF908((W)R) and the BF909((W)R), BF1102(R) are MOSFETs with relatively high transconductance ($Y_{fs\ typ}$ ~ 43 mS) and capacitances ($C_{is\ typ}$ ~ 3.1 - 3.6 pF). The BF1100((W)R), BF1101((W)R), BF1105((W)R) and BF1109((W)R), are MOSFETs with a transconductance between the above mentioned values ($Y_{fs\ typ}$ ~ 28 - 31 mS) and still has low capacitances ($C_{is\ typ}$ ~ 2.2 pF). The MOSFETs were developed with different transferconductances to optimize them for different frequency ranges.The BF1201((W)R), ($Y_{fs\ typ}$ ~ 28mS; $C_{is\ typ}$ ~ 2.6 pF) and BF1202((W)R), ($Y_{fs\ typ}$ ~ 30mS; $C_{is\ typ}$ ~ 1.7 pF) had been especially developed for improved cross-modulation and improved slope of the AGC characteristics.

2. **Dual Devices in Single Packages**

The (2-in-1 MOSFET) BF1102 is a combination of two BF909s with shared source and gate 2 leads. The (2-in-1 MOSFET) BF1203 is a combination of BF1201 and BF1202 with shared source and gate 2 leads.
The (2-in-1 MOSFET) BF1204 is a combination of 2 x BF1202 with shared source and gate 2 leads.

3. **GENERAL**

In the introduction all the type numbers and the different packages are mentioned. The package has no influence on the DC biasing. The influence of the package on the RF parameters (in the frequency area of television tuners) is small. Therefore in this report the application differences and examples will be given for the devices in the SOT143 package. This application information is also valid for the MOSFETs in SOT143R, SOT343R and SOT363.

4. **DC BIAS CIRCUITS**

DC bias circuits for MOSFETs without integrated bias.

We have two basic types of MOSFETs without integrated bias, BF908 and BF998. These MOSFETs are depletion types. Depletion type MOSFETs have negative pinch-off voltages. In TV tuners AGC is necessary. For TV tuners no negative AGC voltaes are available. Due to this lack of negative voltage it is necessary to lift up the source voltage. Otherwise it is not possible to obtain maximum possible gain reduction. This lift up must be done with two resistors in the device source. For AC these resistors must be decoupled with a capacitor. The nominal current of the BF998 is 10mA and that of the BF908 is 15mA. This biasing is done with a voltage divider at Gate1. Because there is no Gate1 current in the MOSFETs the values of the resistors of the Gate1 voltage divider need to be only relatively high resistance. The parallel connection of the 2 esistors should be higher than 10kΩ. The DC circuit for biasing the MOSFETs without integrated bias is then as shown in Fig. 1 below.

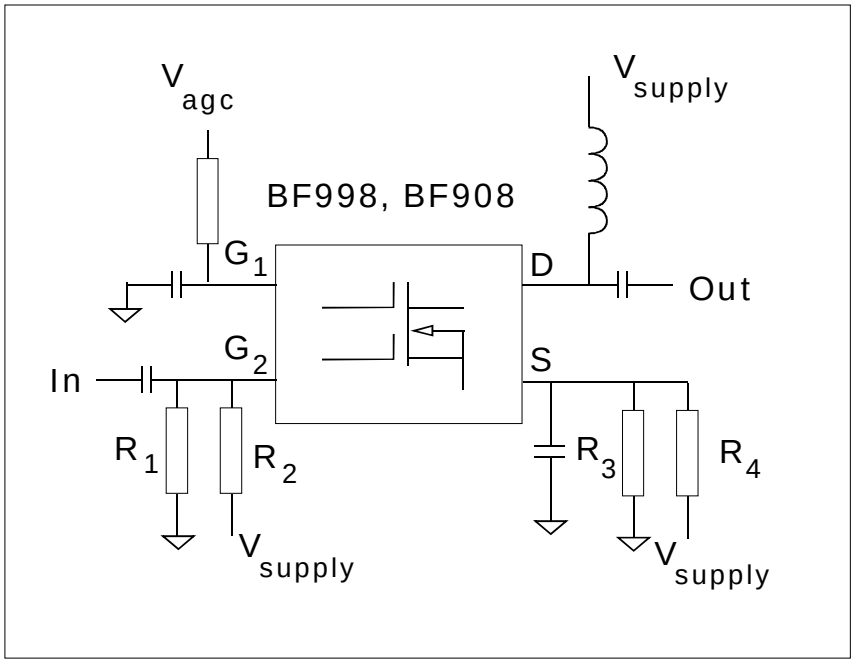


Fig.1: Principle of the bias circuit for MOSFETs without integrated bias.

As stated in the introduction the BF998 and BF908 are for 12V tuners. However, they can be applied at 9V with some loss of performance. For the 12V and 9V application the values of the resistors R_1, R_2, R_3 and R_4 can be calculated. At 12V application we assume that the nominal AGC voltage is 9V. In the 9V application the nominal

AGC voltage is 7.5V. The nominal $V_{G2\text{-}S}$ in the 12V - as well as in the 9V application is 4V. In Table 1 below, the values of the resistors for the 12V- and 9V applications of the BF998 and BF908 are given.

Table 1: Resistors in the bias circuit for MOSFETs without integrated bias.

	V_{supply}	$V_{agc\ nom}$	$V_{G2\text{-}S\ nom}$	$I_{D\ nom}$	R_1 / R_2	R_3 (Ω)	R_4 (Ω)
BF998	12 V	9 V	4 V	10 mA	5 / 7	360	1800
BF998	9 V	7.5 V	4.V	10 mA	7 / 11	240	1200
BF908	12 V	9V	4 V	15 mA	5 / 7	240	1200
BF908	9 V	7.5 V	4 V	15 mA	7 / 11	160	750

DC bias circuit of MOSFETs with partly integrated bias.

We have nine types of MOSFETs with partly integrated bias. The 5V types BF904, BF909, BF1101, BF1102, BF1201, BF1202, BF1203 and BF1204 and the 9V to 12V type BF1100. These MOSFETs are enhancement types. This term means that the pinch-off voltages are positive. No negative voltages are needed for fully switching-off the MOSFETs. Due to this it is not necessary to lift up the Source voltage. For applications of these types the nominal Gate2 voltage is set to 4V.
In 12V applications the nominal AGC voltage is 9V. In a 9V application the nominal AGC voltage is 7.5V. For these applications a voltage divider at Gate2 is needed. Because there is no Gate2 current, no special requirements for this divider are necessary. We propose to set the nominal current of the BF904 and BF1100 at 10mA. That of the BF909, BF1102 and BF1201 at 15mA and that of the BF1101 and BF1202 at 12mA. In the BF1203 we propose to bias the BF1203a at 15mA. We propose to bias the BF1203b, in the BF1203, at 12mA. In the BF1204, we propose to bias both MOSFETs, BF1204a and BF1204b at 12mA. This biasing is done with a resistor (R_{GG}) at Gate1.

The principle of the DC circuit biasing for MOSFETs with partly integrated bias is as given in Figures 2 and 3 (next page).

Note: In Figures 2 and 3 the basic principles of the circuit are given. There is no information about the pin-outs of the different MOSFETs. The pinning of the BF1204 is different from that of the BF1102 and BF1203.

The necessary resistors for the different applications are given in Table 2 (page 5).

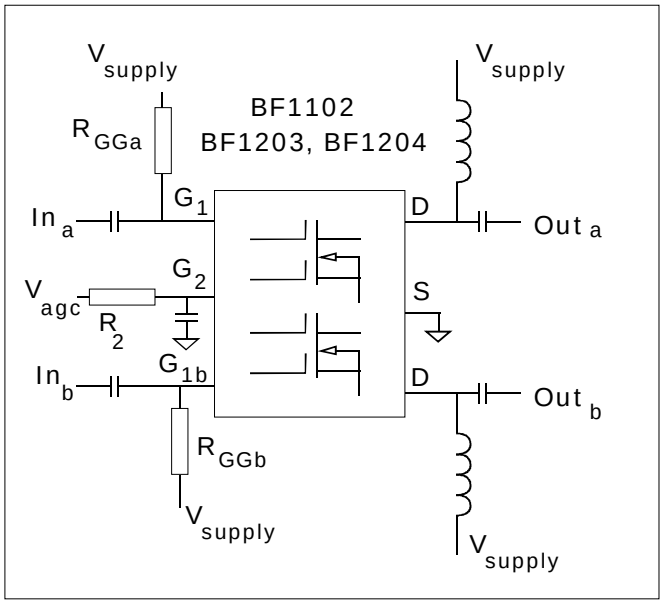


Figure 2: Basic bias circuit for single MOSFETs with partly integrated bias.

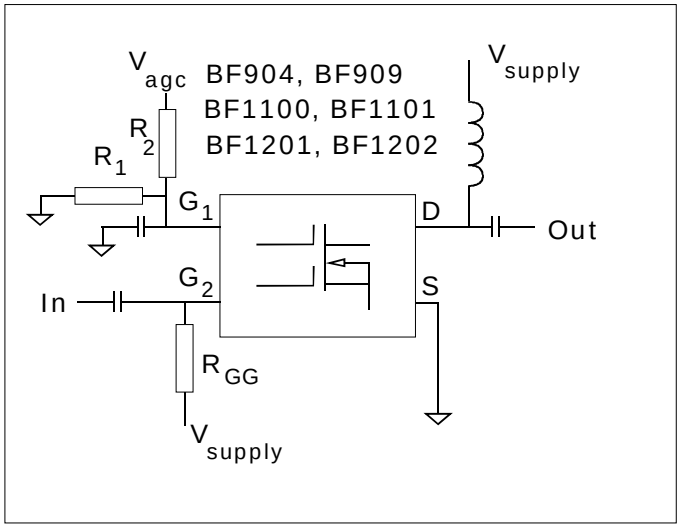


Figure 3: Basic bias circuit for dual MOSFETs with partly integrated bias.

Table 2: Resistors in the bias circuit for MOSFETs with partly integrated bias.

	Application	Proposed I_D	R_{GG}	R_1 / R_2
BF904	5 V	10 mA	120 kΩ	no R_1
BF909	5 V	15 mA	120 kΩ	no R_1
BF1101	5 V	12 mA	120 kΩ	no R_1
BF1100	9 V 12 V	12 mA 12 mA	180 kΩ 250 kΩ	8 / 7 4 / 5
BF1201	5 V	15 mA	62 kΩ	no R_1
BF1202	5 V	12 mA	120 kΩ	no R_1
BF1102 (1)	5 V	15 mA	120 kΩ	no R_1
BF1102 (2)	5 V	15 mA	120 kΩ	no R_1
BF1203a	5 V	15 mA	62 kΩ	no R_1
BF1203b	5 V	12 mA	120 kΩ	no R_1
BF1204a	5 V	12 mA	120 kΩ	no R_1
BF1204b	5 V	12 mA	120 kΩ	no R_1

DC bias circuit of MOSFETs with fully integrated bias.

We have two types of MOSFETs with fully integrated bias. The 5V type BF1105 and the 9V type BF1109. These MOSFETs are also enhancement types and therefore no negative voltages are needed for fully switching-off the MOSFETs. Due to this it is not necessary to raise the source voltage above ground reference. Because of the fully integrated bias no external resistor at Gate1 is needed for biasing the MOSFETs. Both types, BF1105 and BF1109, have been developed for a typical "Self Biasing Current" of 12mA.

For application of these types the nominal Gate2-Source voltage is to be set to 4V. In 5V applications the nominal AGC voltage is 4V. In a 9V application the nominal AGC voltage is 7.5V. For the 9V application a voltage divider at Gate2 is needed. Because there is no Gate2 current, no special requirements for this divider are necessary. The DC circuit for biasing the MOSFETs with fully integrated bias is shown in Figure 4 (next page).

The necessary resistors for the different applications are provided in Table 3 (below).

Table 3: Resistors in the bias circuit for MOSFETs with fully integrated bias.

	Application	Typical "Self biasing current"	R_1 / R_2
BF1105	5 V	12 mA	no R_1
BF1109	9 V	12 mA	8 / 7

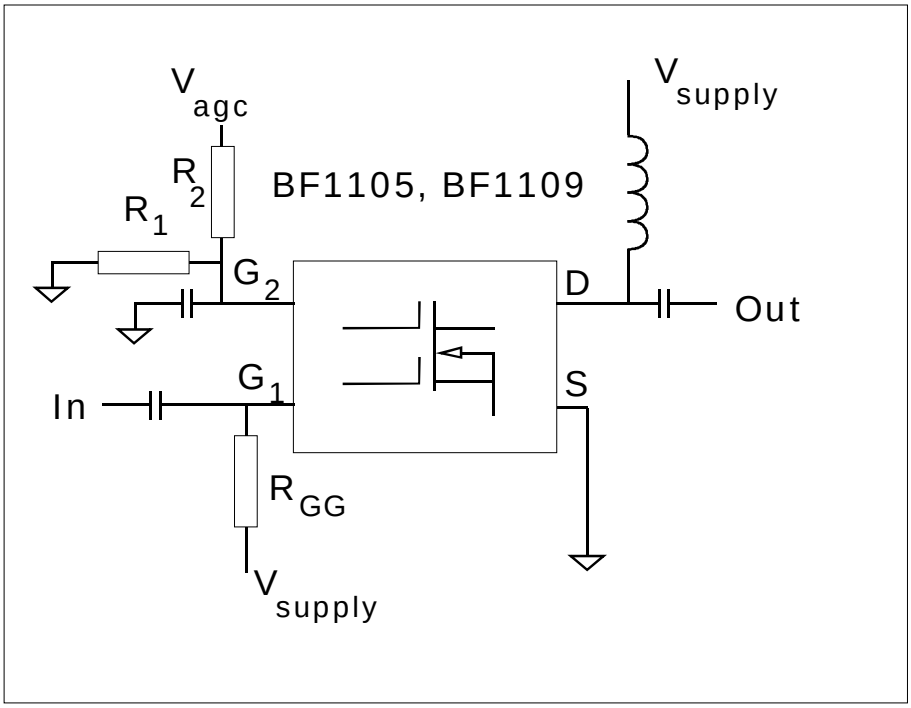
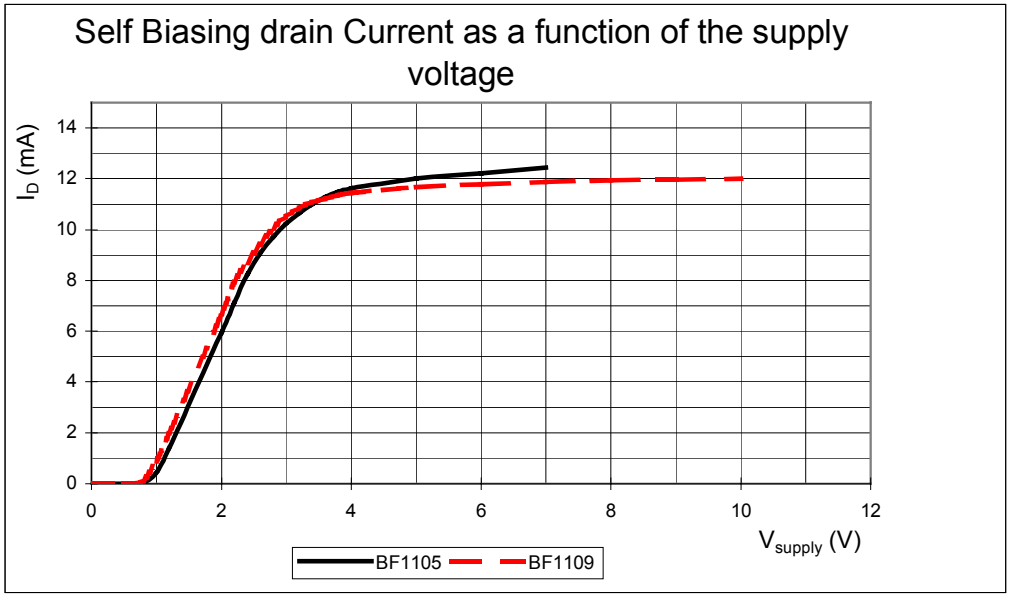


Fig. 4: Principle of the bias circuit for MOSFETs with fully integrated bias.

The self-biasing current of the BF1105 and BF1109 are, over a large range of the supply voltage, only marginally
dependent on the supply voltage. The relation between the self-biasing current of the BF1105 and BF1109, and the supply voltage is given in Graph 1 (below).



Graph 1.

AGC CHARACTERISTICS

The AGC characteristics of the different MOSFETs are measured in the AC circuit as given in Fig.5.

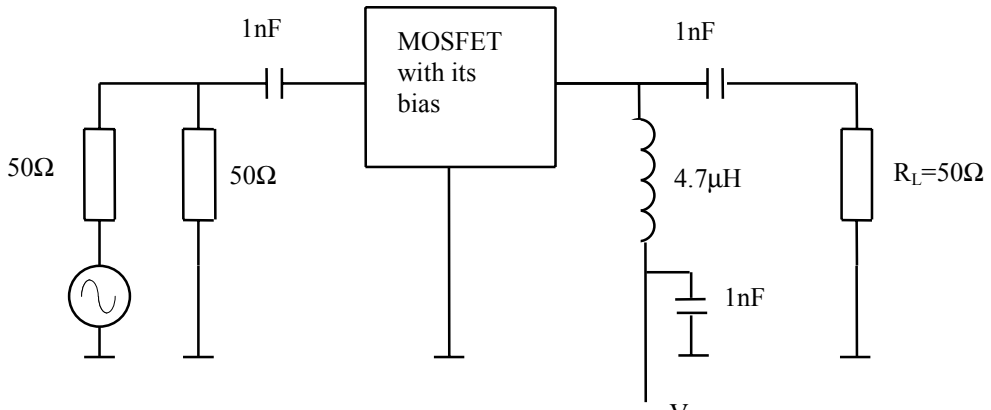
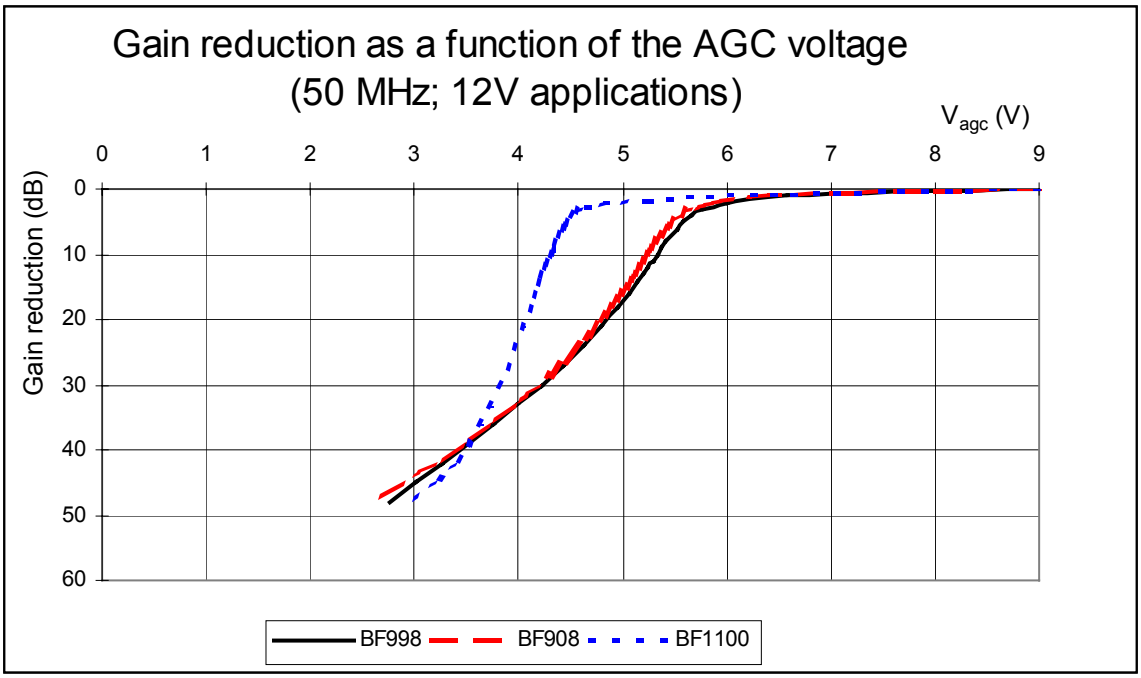


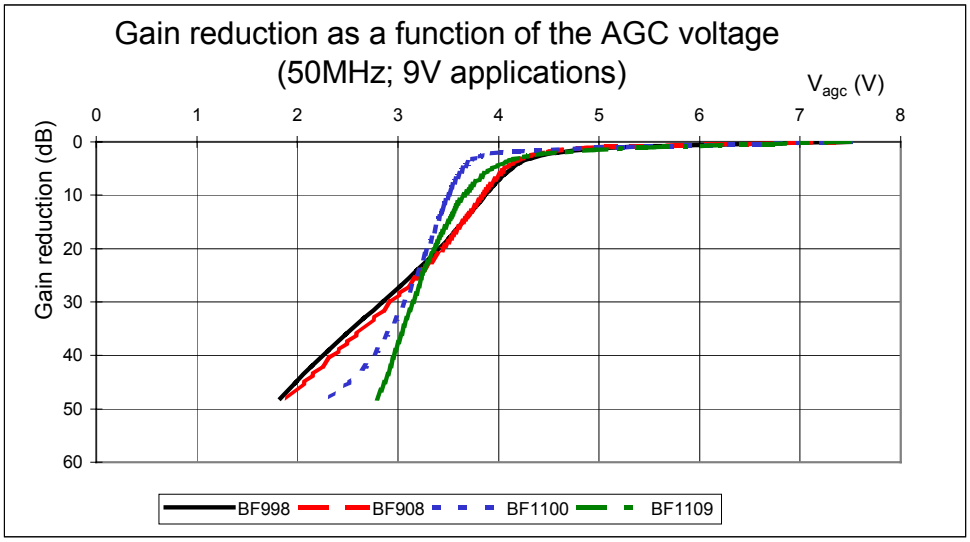
Figure 5: AGC and Cross-modulation Test

The DC bias circuits for the different MOSFETs were discussed in chapter 3. For 12V applications the nominal AGC voltage was chosen as 9V, for 9V applications the choice was 7.5V and for 5V appli-cations the choice was 4V. All MOSFETs are characterized at 50MHz. The results of these measure-ments are given in the **Graph 2** (12V application), **Graph 3** (9V application) and **Graph 4** (5V application). From these graphs we see that the MOSFETs with partly and fully integrated bias have a steeper AGC characteristics than MOSFETs without integrated bias.



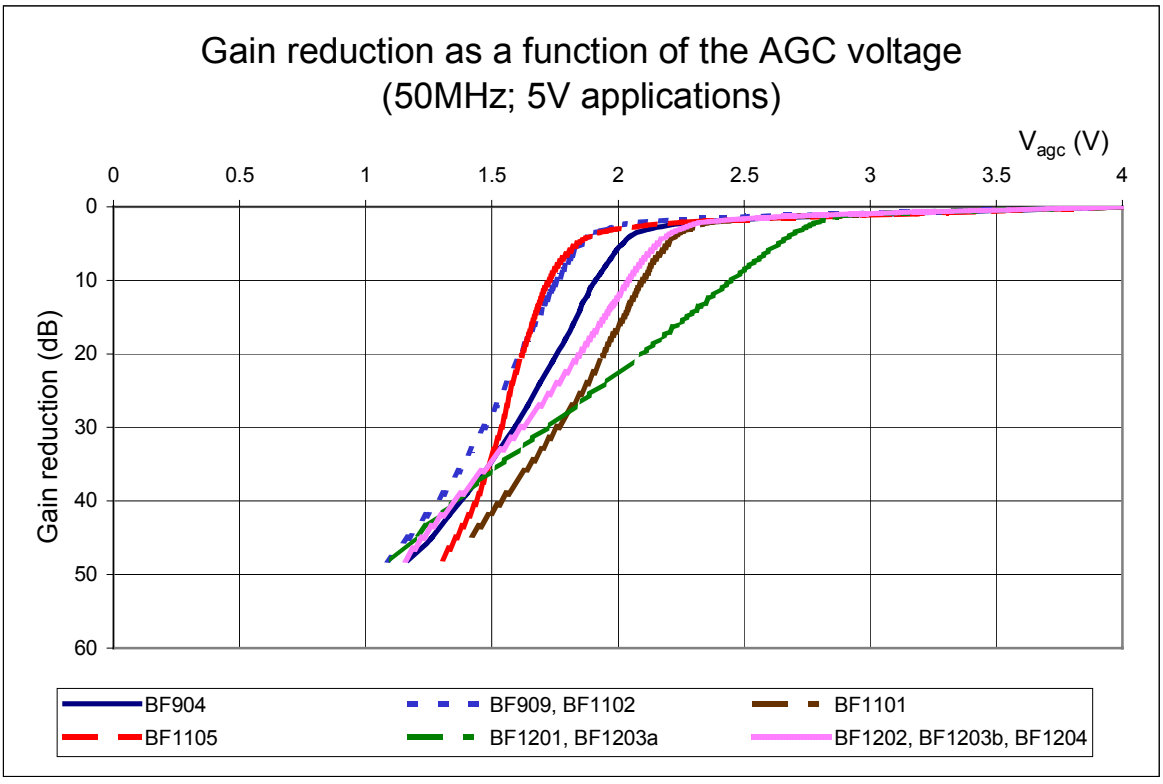
Graph 2 12 Volt Applications

Graph 3 9 Volt Applications



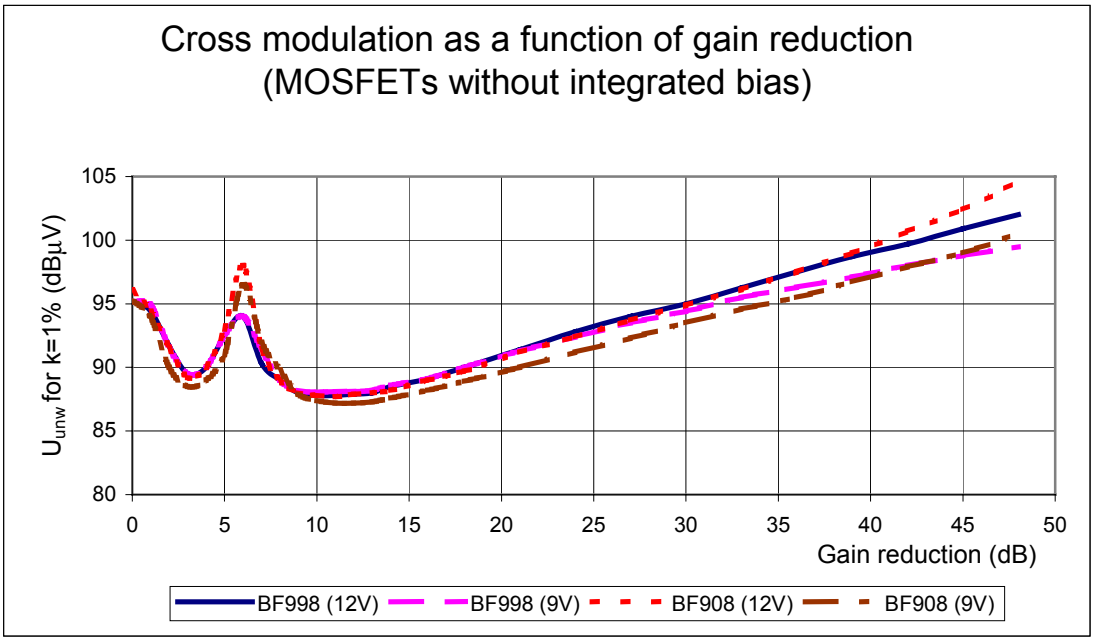
Graph 4 5 Volt Applications

From Graph 4 we see clearly the improvement of the AGC characteristics of the BF1201, (BF1203a) and the BF1202, (BF1203b and BF1204), especially the BF1201 (BF1203a).



5. **CROSS-MODULATION PERFORMANCE**

The cross-modulation performance was measured in a circuit of the basics of which are given in Figure 5. The results of the cross-modulation measurements in the circuit of Fig.5 are given in the Graphs 5, 6, and 7. Graph 5 shows the cross-modulation performance of the MOSFETs without integrated bias.



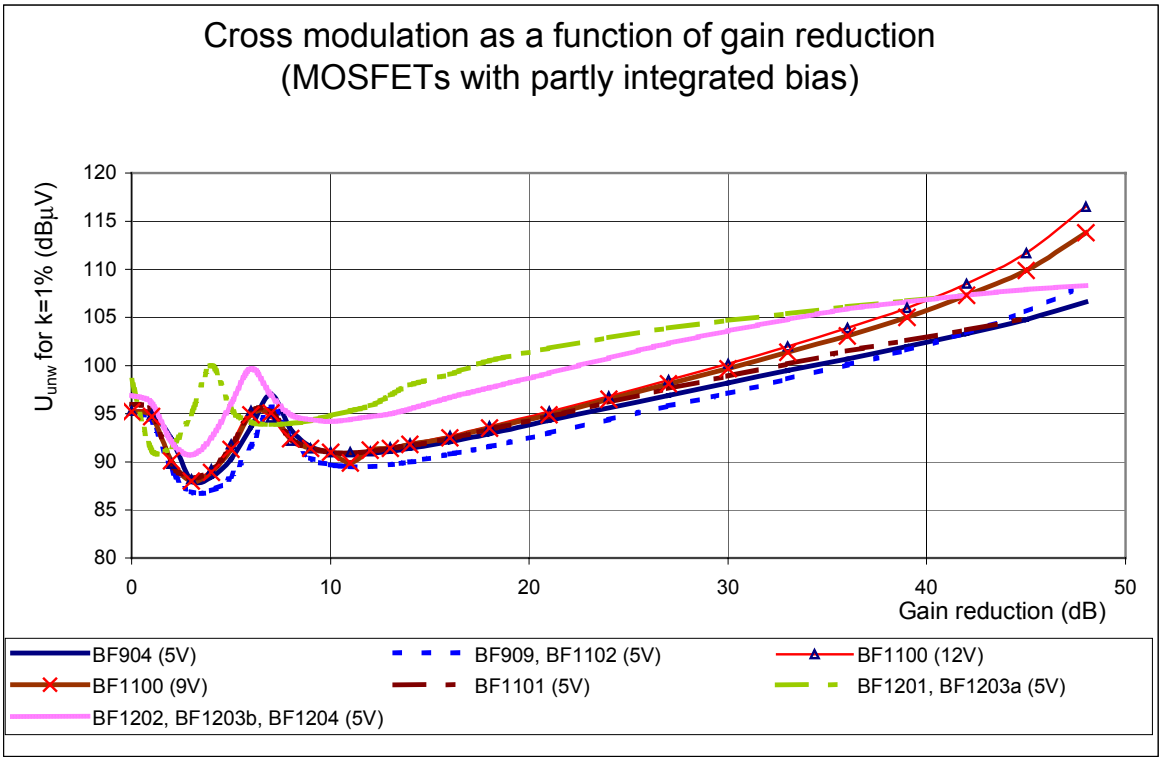
Graph 5

The difference in the curves of the BF998 and BF908 (at gain reduction > 40dB) is caused by internal capacitances. Internal capacitances of the BF908 are higher than that of the BF998. Due to this the cross-modulation performance after 40 dB gain reduction is increased.

Note: Series inductance in the Source has the same effect as increasing the internal capacitances.

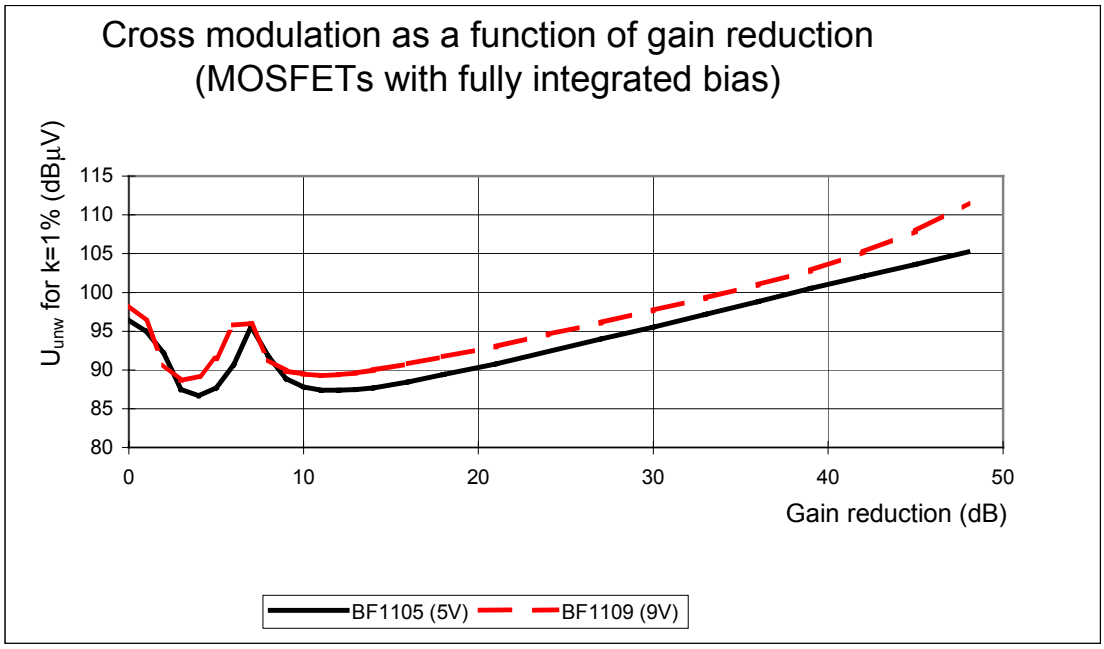
The difference in the performance at 12V and 9V supply voltages are caused by the difference in effective Source resistor. Due to this effective Source resistor the Gate1 - Source voltage increases (during AGC) 3V in a 12V application and only 2V in a 9V application. The higher this voltage-increase, the better the cross-modulation performance.

Graph 6 (next page) shows the cross-modulation performance of the MOSFETs with partly integrated bias. The differences we see here are caused by the different increase of the Gate1 - Source voltage during AGC, caused by the different supply voltages. For the MOSFETs in a 5V application the Gate1 - Source voltage at maximum gain reduction is 5V. For the BF1100 the Gate1 - Source voltage at maximum gain reduction is 9V in a 9V application and 12V in a 12V application. The BF1201 (BF1203a) and BF1202 (BF1203b and BF1204), are especially developed for improved cross modulation. This can clearly been seen from the characteristics.



Graph 6

Graph 7



CONCLUSIONS

For the modern 9V and 5V applications we recommend the use the MOSFETs with partly and fullyintegrated bias. This allows fewer external components for biasing. The advantage of MOSFETs with partly integrated bias is that these devices can be used at different voltages and different drain currents. The BF1100 can be applied at supply voltages between 9V and 12V. All 5V MOSFETs with partly integrated bias can be applied at supply voltages between 3V and 7V.

It must be taken into account that if the supply voltage is chosen below 5V, the nominal AGC voltage should be chosen at least 0.5V lower than the supply voltage.

The advantage of MOSFETs with fully integrated bias is that the "self biasing" current over a relatively large range of the supply voltage is almost independent on this supply voltage.

The slope of the AGC characteristics of the BF1201 (BF1203a) and BF1202 (BF1203b and BF1204) is much less steep than that of the other partly- or fully-internally biased MOSFETs. The cross modulation performance of the BF1201 (BF1203a) and BF1202 (BF1203b and BF1204) is much better than that of the other 5V MOSFETs, especially in the region between 10dB and 30dB gain reduction.

Appendix F: Application note
WCDMA appl.: BGA6589 Wideband Amplifier

1.0 Introduction.
This application note provides information that is supplementary to the data sheet for the BGA6589 amplifier, and includes temperature and DC stability characteristics and WCDMA information.

Figure 1 shows the biasing method. The device is matched to 50 ohms.

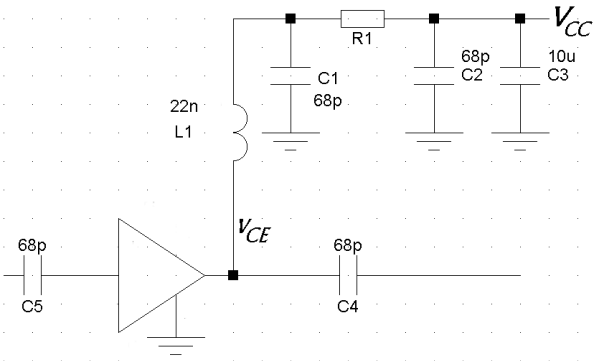


Figure 1. Bias Method.

2.0. DC Characteristics.
Figure 2 shows the DC load line characteristics of the device, when biased with two different voltage and resistor combinations.

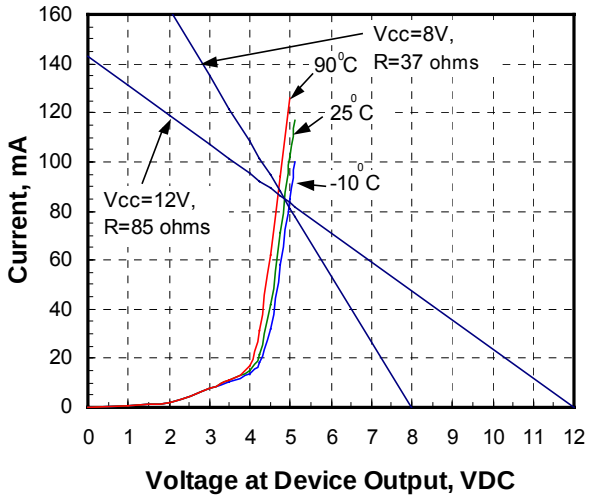


Figure 2. BGA6589 DC Characteristics.

Reviewing the graphical load line method, we superimpose the equation for the load resistor onto the device characteristics, and the intersection shows the current and the voltage of the device. The equation for the resistor is basically a horizontally flipped version of a straight line representing a resistor across a voltage source, which of course runs through the origin and has a slope determined by *R* and *V*.

Using BJT terminology, the device voltage at the output pin is $V_{CE.}$ and the supply is V_{CC}.
Then,

$$v_{CE} = V_{CC} - Ri_C \quad \text{and}$$

$$i_C = \frac{V_{CC}}{R} - \frac{v_{CE}}{R} = I_O - \frac{v_{CE}}{R}$$

where *Io* is the intercept on the y axis.

Figure 3 shows the same data expanded. We can see that when biasing with 8V and 37 ohms, the current is stable over temperature from 82 to 89 mA.

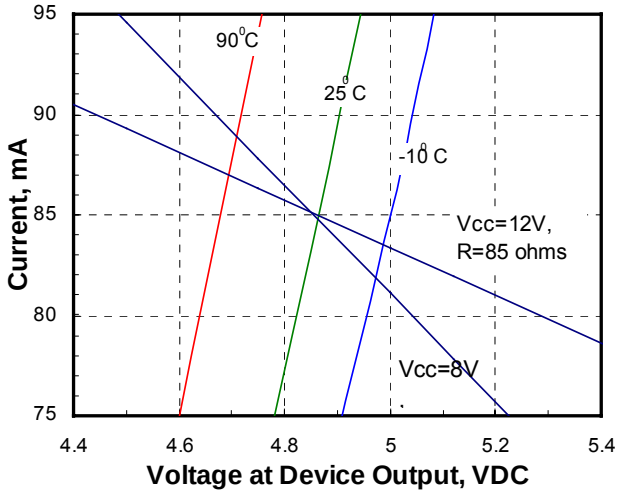


Figure 3. DC Characteristics Expanded

Device variations, however small, and supply voltage variations are not yet accounted for in the figure. However, when we look at how the device functions at different currents, we see that I_C is not critical. For example, in Figure 4 we see that the gain is virtually independent of the bias current.

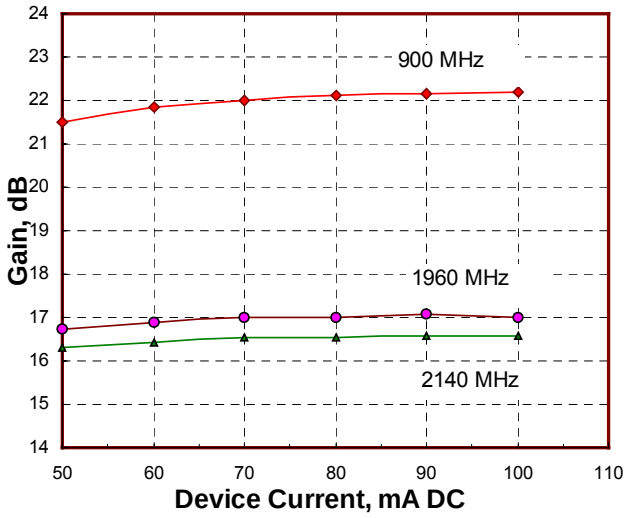


Figure 4. Gain Stability with Bias.

Similarly, the gain vs. temperature is shown in Figure 5. There is a slight negative temperature coefficient.

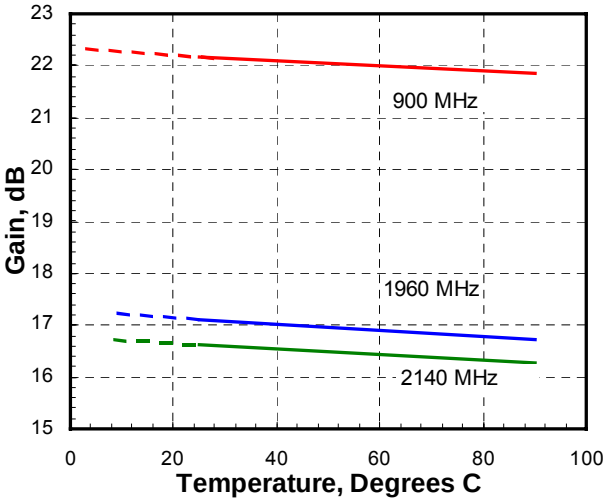


Figure 5. Gain Stability with Temperature.

3.0. WCDMA Performance.

3.1. Normal Bias. Figure 6 shows the spectrum for WCDMA 3GPP, with 15 channels of data. The frequency limits for measurement are shown by the arrows for the reference (on) channel and the adjacent channel. The channel powers are integrated over a 3.84 MHz band, with a channel offset of 5 MHz for the ACP measurement.

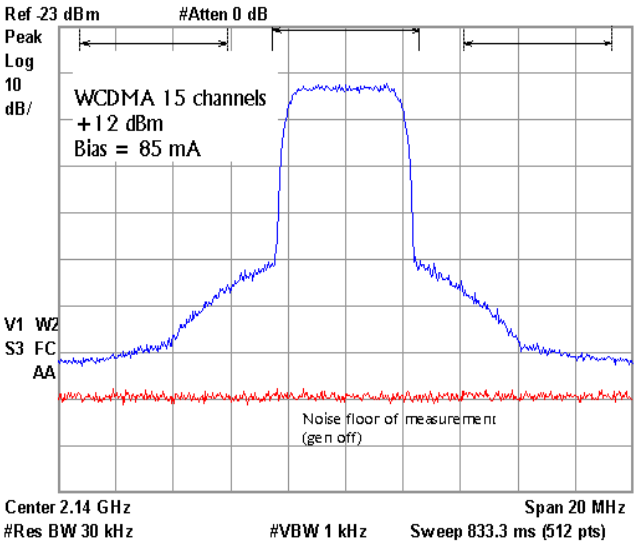
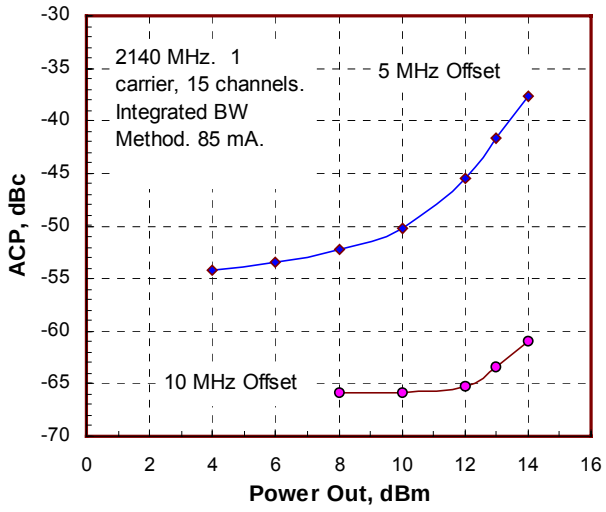


Figure 6. WCDMA Spectrum.

Figure 7 shows the 5 and 10 MHz offset measurements over a power range. There are many parameters that affect the ACP, even for the same number of channels and their allocations, such as the data type (random or repeating), the powers in the channels (equal or different), pilot length, timing sequence, and the symbol rate.



The effect of the number of data channels in the WCDMA signal is shown in Figure 8.

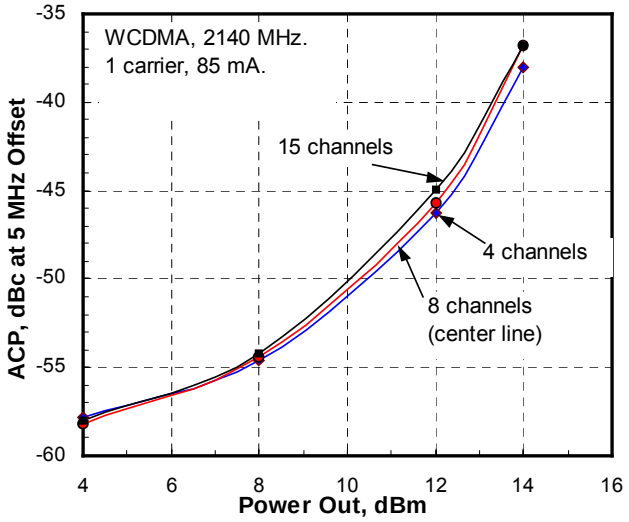


Figure 8. Effect of Number of Data Channels.

3.2. Reduced Bias. The compression point (P1dB) is affected by the device current, as expected. The effect of the current and the associated P1dB on the WCDMA performance is shown in Figure 9. At low powers, the device can tolerate a lower current and still stay within acceptable limits. At +12 dBm, the bias can drop to 75 mA without undue degradation.

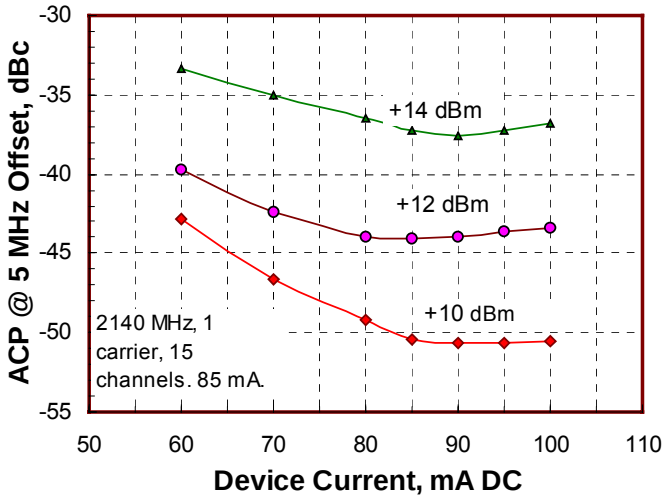


Figure 9. ACP with Reduced Bias.

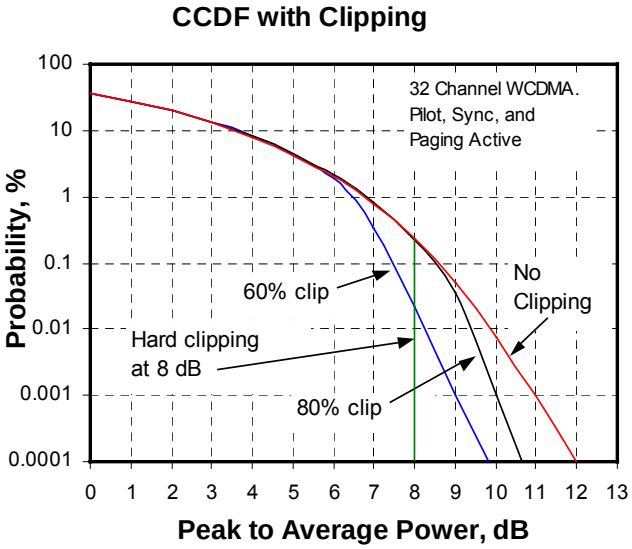


Figure 10. CCDF.

4.1. CCDF. In WCDMA systems (and IS95 systems and QAM systems in general), the peak to average ratio of the signal can be 12 dB or more. In an amplifier application, designing in enough headroom to handle all the peaks would make it unnecessarily expensive and inefficient. The highest peaks only occur a small portion of the time (such as parts per million), and can be allowed to compress in the amplifier. The trade-off is of course distortion and ACP.

A complementary cumulative density function (CCDF) curve is shown in Figure 10 for 32 data channels. Consider first the CCDF for the case of no clipping. As a very rough thumbnail estimate of ACP, we know from analysis that limiting or clipping of events that happen .01% of the time can cause ACP's in the general range of –40 dBc. This of course is dependent on many factors, such as type of limiting (hard clipping vs. soft compression, etc.). The value of –40 dBc corresponds to 10 log (.0001), where .0001 is simply .01% as a fraction.

4.2. Digital Hard Clipping. In the physical layer of WCDMA systems, advantage can be taken of the high level of redundancy in the coding, spreading, and overhead bits of the basic channel data by eliminating some of the symbols before entering the amplifier/transmitter. The air interface is designed to operate with fading, dropouts, static etc., therefore, eliminating some small percentage of the symbols can be tolerated, because the bulk of these symbols are corrected for in the receive decoding process.

In the basestation, this clipping is done on the digital summation of all the I and Q samples, *before filtering.* This is critical. This way, the ACP energy caused by the clipping can be filtered out in the baseband filters before amplification. The filtering process softens up the CCDF curve that would otherwise be a hard clip, an example of which is shown in Figure 10.

Also in Figure 10, the CCDF is shown for the cases of clipping the signal at 60% and 80% relative to the highest peak, followed by filtering. While this may seem to be a severe amount of clipping, the highest peaks (uncommon as they are) might actually be 14 dB or more above the average power, so the more typical peaks of 10 dB or so are not clipped very much.

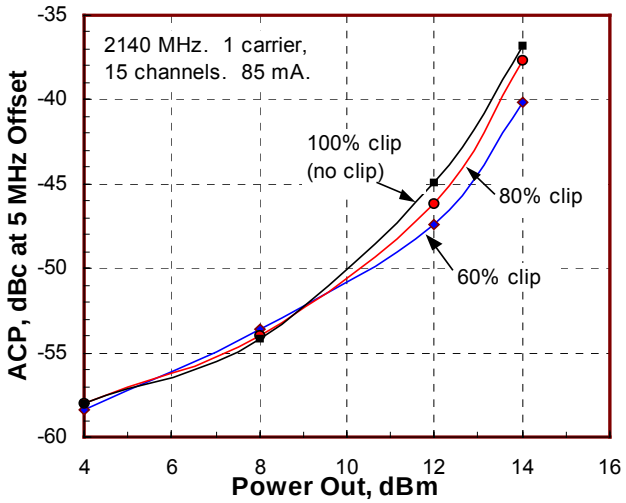
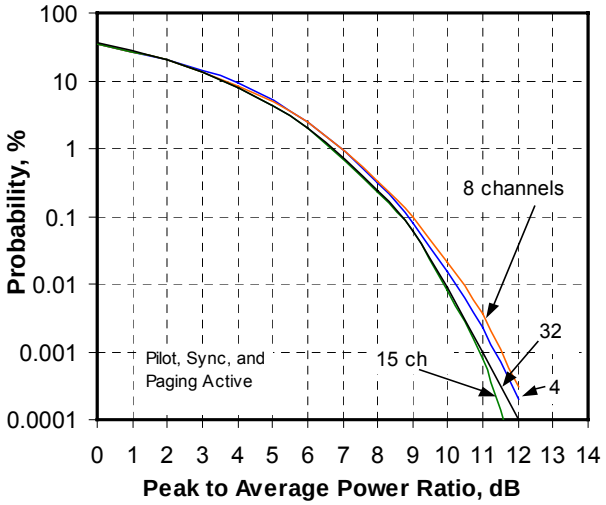


Figure 11. Clipping effects on the ACP.



The effect of clipping on the ACP is shown in Figure 11, for a 15 channel WCDMA signal. This is measured data for the BGA6589. The x axis is average power.

For 32 channels, the ACP is very similar, because the CCDFs are similar, as shown in Figure 12.

5.0. Load Pull.

Class A devices are not often subjected to a load pull test, but doing so shows the resiliency of the device when the BGA6589 is feeding a stage with a less than perfect S11. Figure 13 shows the ACP under various VSWR conditions.

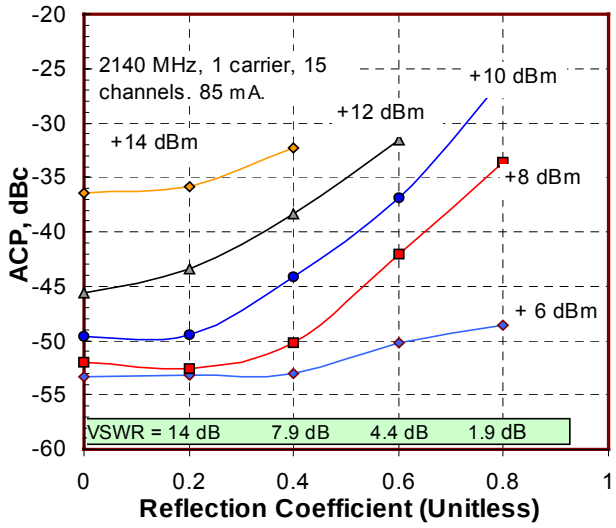


Figure 13. Load Pull Test.

For this test, the worst of four phases of reflection was plotted for a given reflection coefficient, at several powers. The VSWR corresponding to the reflection coefficient is shown just above the x axis. At low/medium powers, a significantly "poor" load reflection is tolerable, before degrading the ACP. For each measurement, the gain necessarily changed due to the loading, and the input drive was changed accordingly to keep the output power constant.